Processing Speed Impact of the Pipeline-Length on a Custom RISC-V CPU for FPGAs

Julian Weihe Timm Bostelmann Sergei Sawitzki

FH Wedel
University of Applied Sciences
Contact: bos@fh-wedel.de

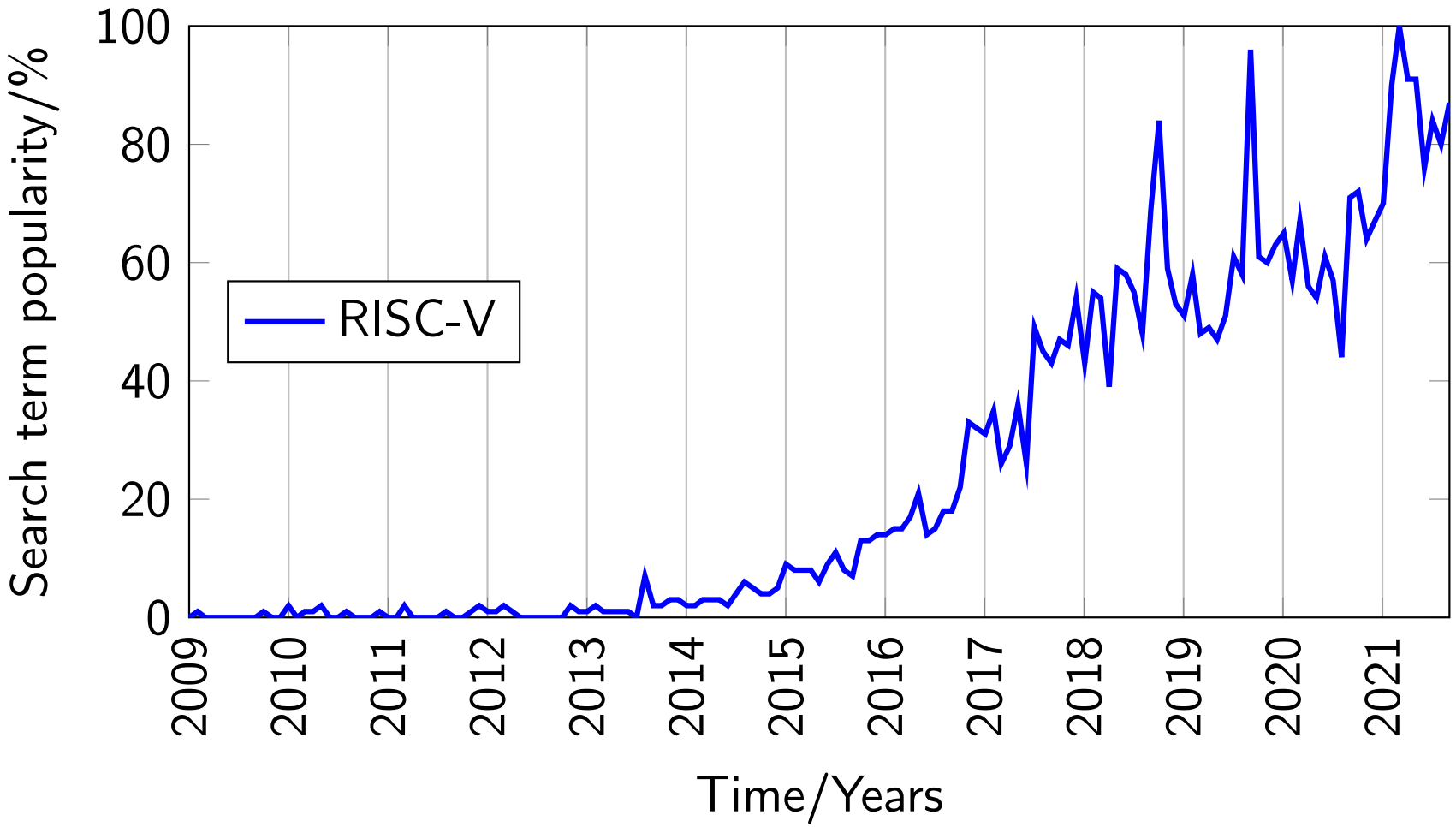
CENICS 2022

Presenter's Resume

Timm Bostelmann received his engineer's degree in computer engineering from the FH Wedel (University of Applied Sciences) in 2008. Since then, he is employed at FH Wedel as a research assistant in the field of embedded systems.

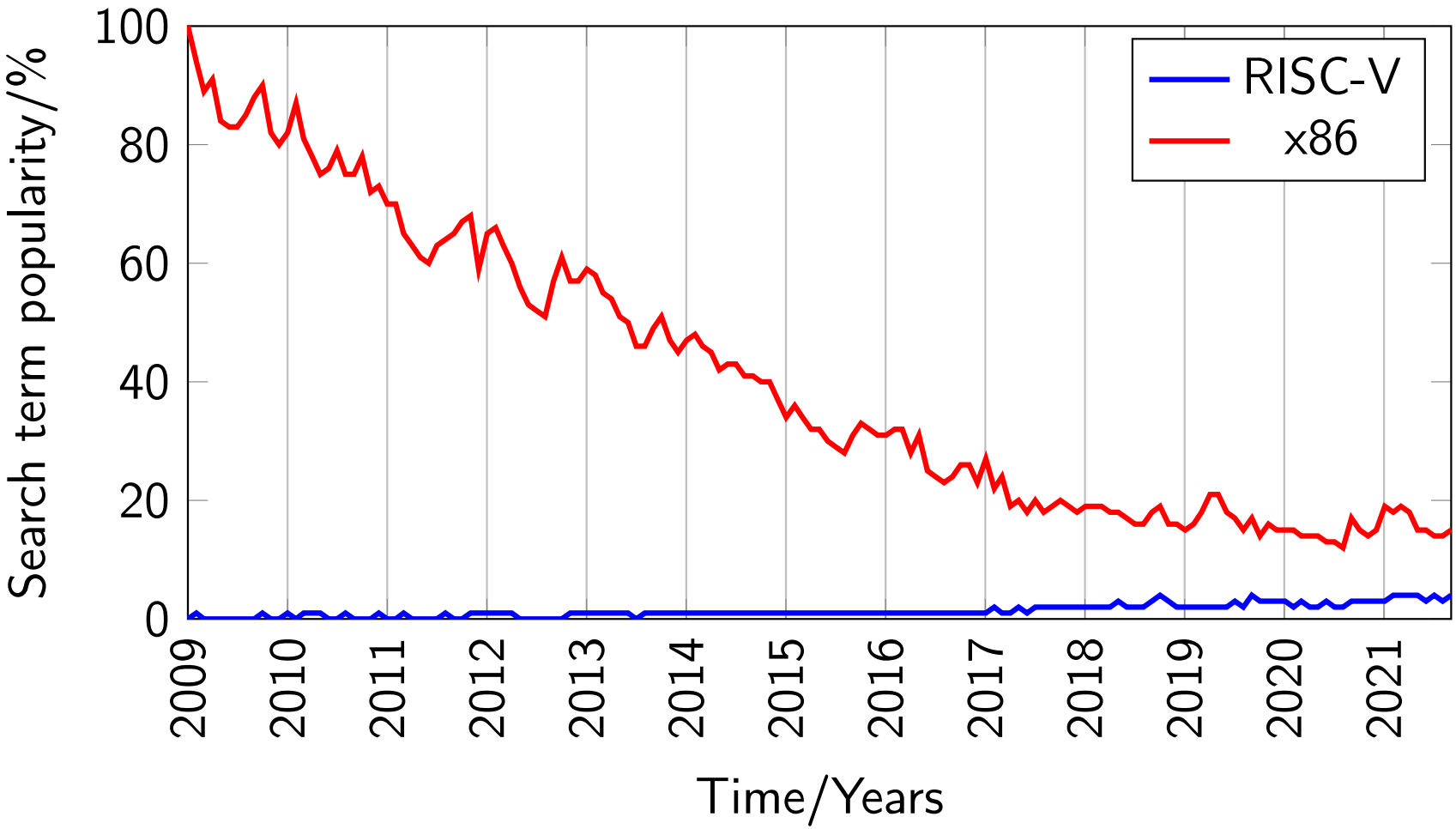
Google Trends

- Popularity by searches for processor architecture "RISC-V".



Google Trends

- Popularity by searches for processor architecture "RISC-V" vs "x86".



Motivation

- Effects of the choice of the number of pipeline stages when implementing an own RISC-V CPU.

Benchmarking using CoreMark

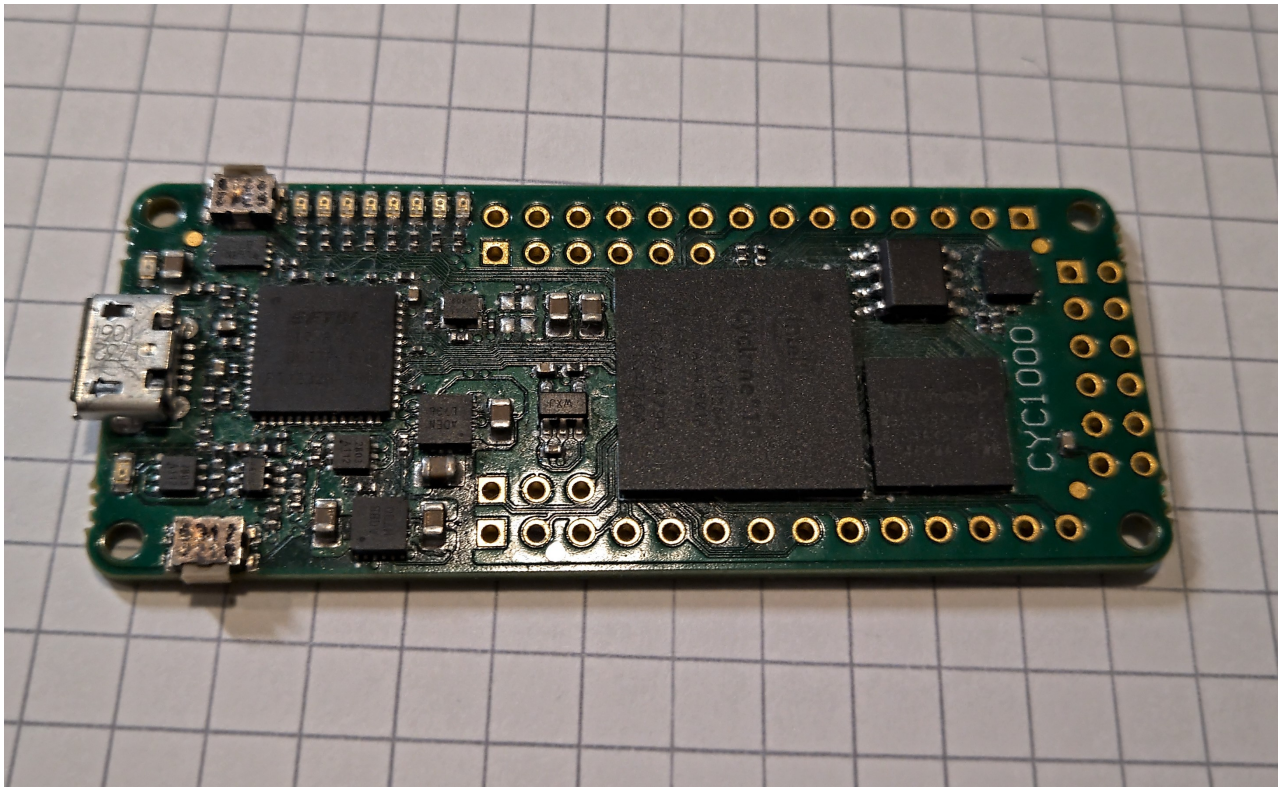
- Developed by EEMBC
- Focus on list processing, matrix operations, state machines and CRC.

Time analysis

- Timing Analyzer in Quartus Prime Lite

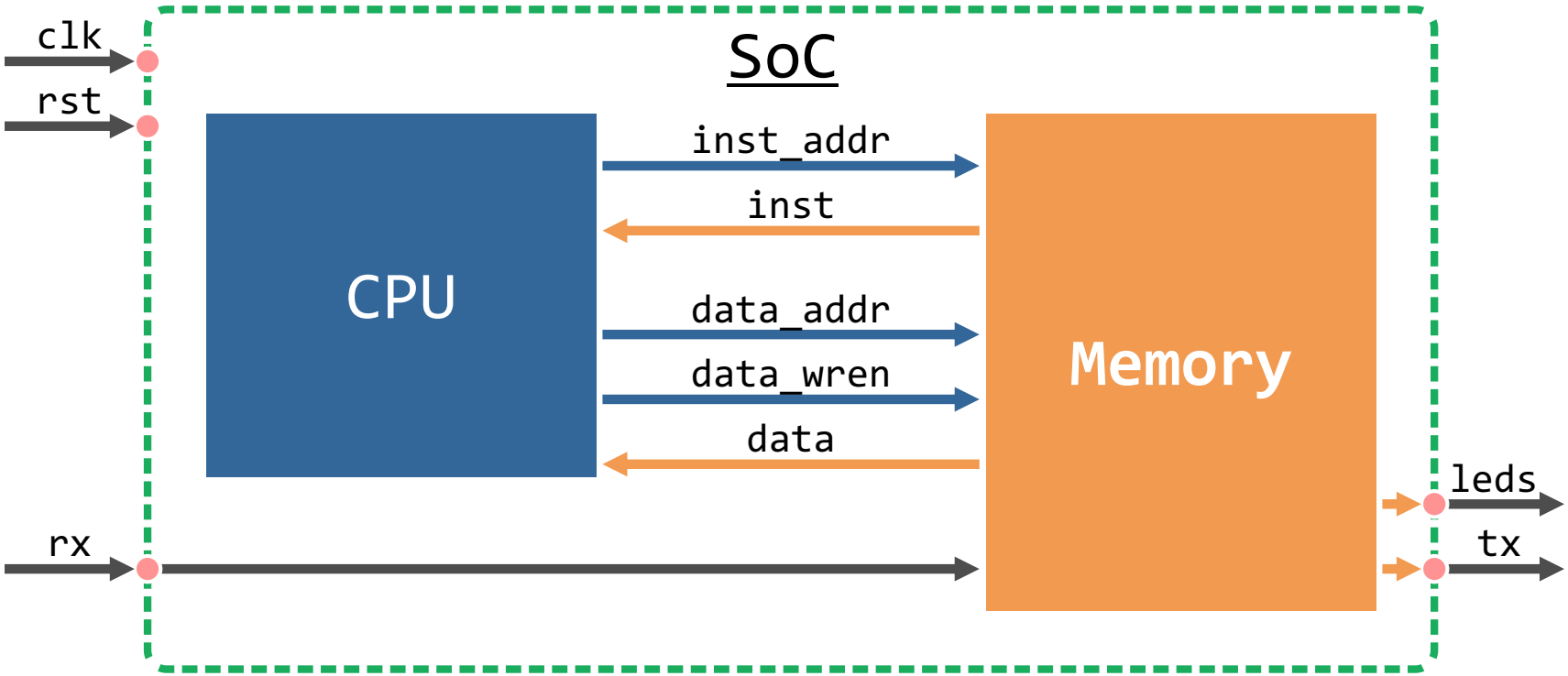
Hardware: Intel Cyclone 10LP 10CL025 FPGA

- 25000 Logic Elements
- 594 Kb embedded Memory (M9K)
- 12 MHz external clock



trenz electronic: CYC1000

CPU environment



- Peripherals are mapped in the memory.
- The implementation of the CPU is independent of the memory.

Pipeline stages

Five-stage CPU

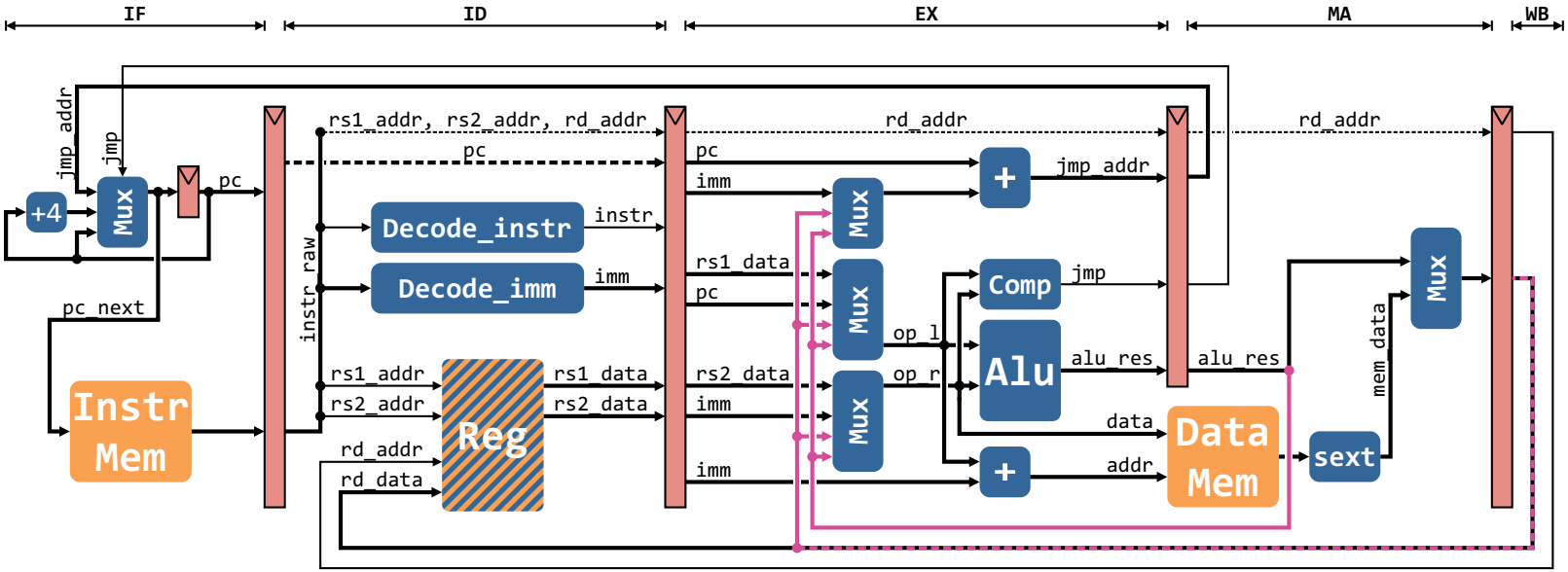
1. IF - Instruction Fetch
2. ID - Instruction Decode
3. EX - Execution
4. MA - Memory Access
5. WB - Write Back

Two-stage CPU

1. IF/ID/EX
2. MA/WB

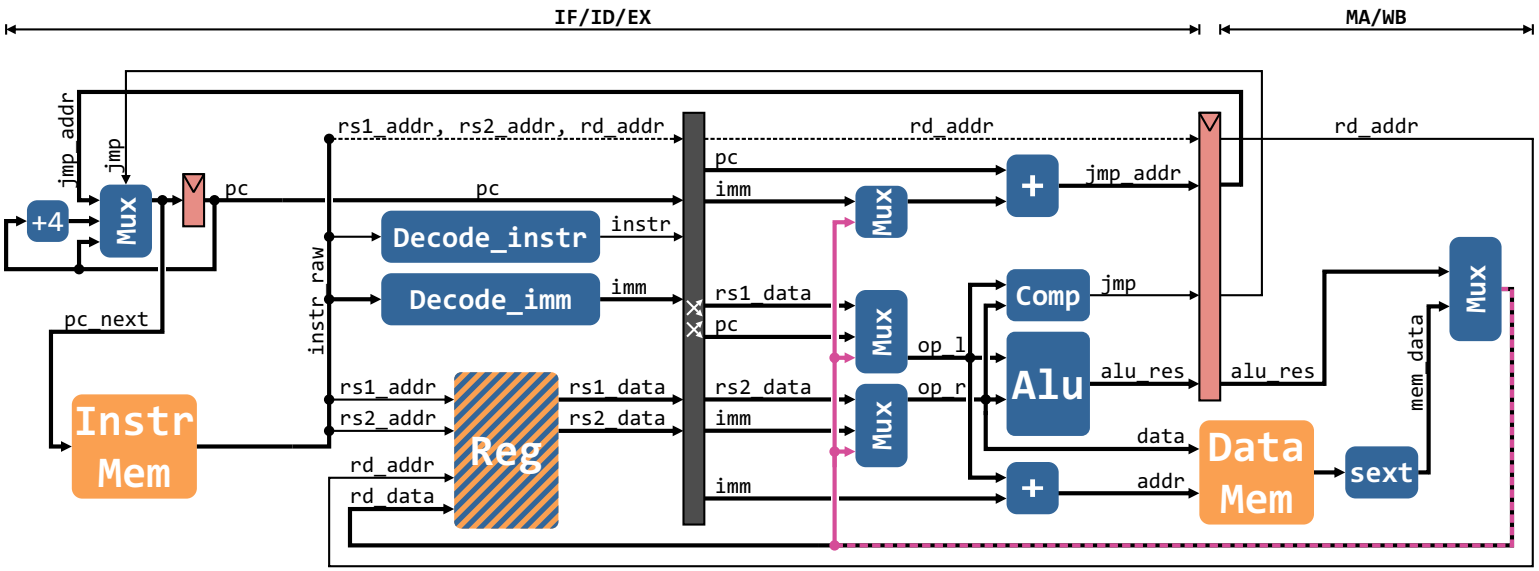
- Two stages are always needed due to the clock controlled data memory access.

Five-stage pipeline CPU



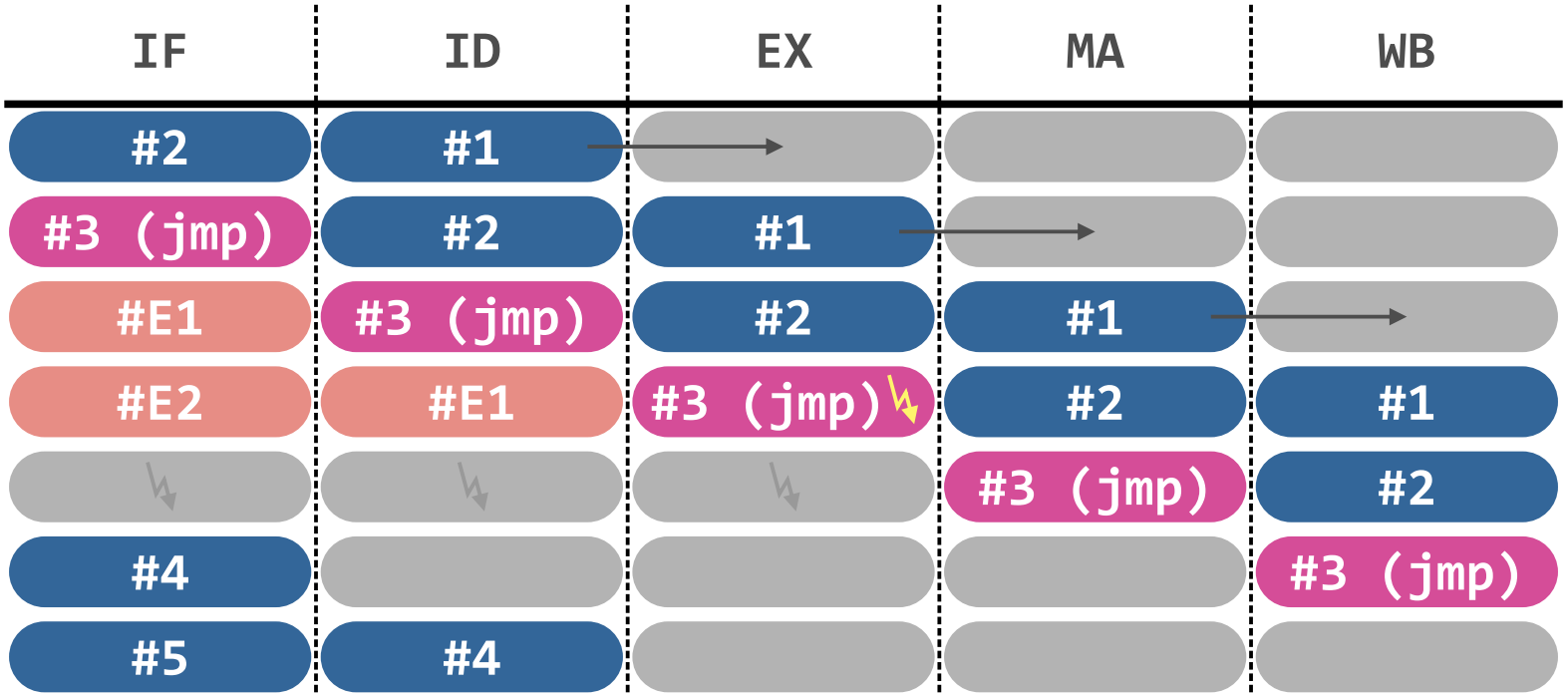
- Implementation of rv32i-ISA.

Two-Stages pipeline CPU



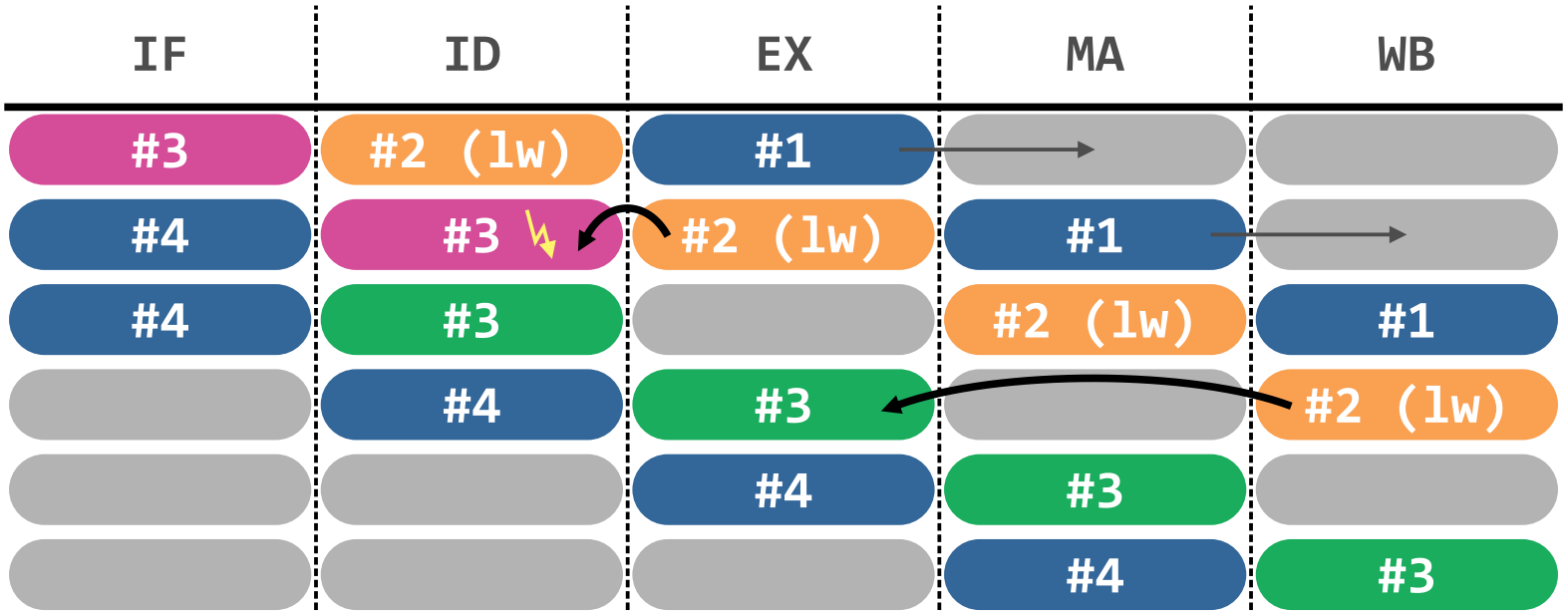
- Implementation of rv32i-ISA.
- Names of the combined stages and structure were taken from the five-stage pipeline CPU.

Jump Instruction Problem



- The jump is registered in the execution stage.
- Instructions that have been read in until this stage are discarded.

Read Memory Instruction Problem



- The Load Word (LW) instruction needs another clock to get the result from the memory.
- A stall-instruction is inserted if the following instruction requires the memory data.

Comparisons

CoreMark Score

- Instructions per clock cycle
- Maximum clock speed
- Calculation of CoreMark-Score:

$$Score_{Iterations\ /\ Sec} = \frac{Iterations \cdot Frequency}{Ticks_{Total}}$$

Space requirement of the additional pipeline stages on FPGA

- Number of additional Logic Blocks
- Number of additional Register

Coremark Scores

Stages	Frequency / MHz	Iterations	Ticks	Score
2	12.000	200	203629411	11,786
2	39.670	200	203629411	38,963
5	12.000	200	247103108	9,7125
5	67.380	200	247103108	54,536

two-stage pipeline CPU

- 21 % more instruction per clock circle

five-stage pipeline CPU

- 70 % higher clock frequency
- 40 % higher CoreMark score

Used space on FPGA

Stages	Optimization mode	Logic Elements	Register
2	Balanced	4566	1344
2	Performance	4769	1577
5	Balanced	4821	1670
5	Performance	5009	1833

Comparison with Performande Optimization

- 1.1 % more Logic Elements
- 1.2 % more Register

Conclusion

- Jumps and memory accesses lead to miscalculations and reduce processing speed (only affects the five-stage CPU).
- Due to the miscalculations, it can no longer be assumed that an instruction is processed in every clock cycle.
- The five-stage pipeline CPU offers a higher clock frequency which results in a higher CoreMark score.
- The additional space requirement is rather marginal.

Recommendation

- For maximum processing speed, the five-stage pipeline CPU is more recommended.
- If super real-time requirements are precise, the two-stage pipeline CPU can also be interesting.