A Comparison of Verilog Synthesis Frontends

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Introduction

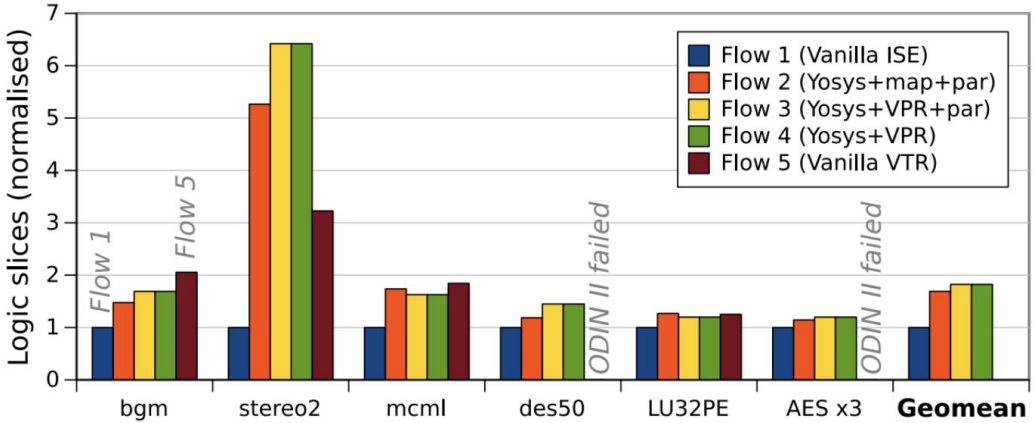
- Comparison of Odin-II and Yosys
- Both Verilog synthesis tools
- Odin-II is part of the Verilog-To-Routing (VTR) project
- Yosys is part of the SymbiFlow project

Motivation

- Field Programmable Gate Arrays (FPGAs) are a versatile tool
  - Useful for rapid prototyping, testing and research
  - More flexible than than Application Specific Integrated Circuits
  - Lower upfront costs
- Open-source flows enables easier research
  - Experimental FPGA designs
  - New synthesis techniques

Existing Work

- Hung* demonstrated that Yosys tends to perform better, but Odin-II is ahead in some aspects
- Missing some runtime metrics
- Significant improvements in both tools since

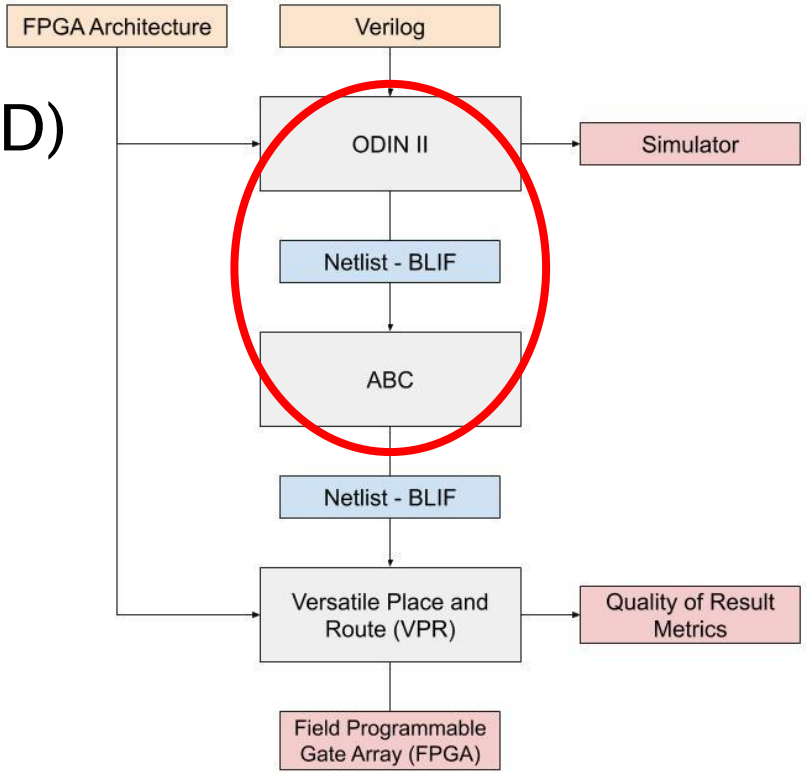


Area Utilisation for a range of Verilog benchmarks. Lower is better.

**E. Hung, "Mind the (synthesis) gap: Examining where academic FPGA tools lag behind industry," 2015 25th International Conference on Field Programmable Logic and Applications (FPL), London, 2015, pp. 1-4, doi: 10.1109/FPL.2015.7294007.*

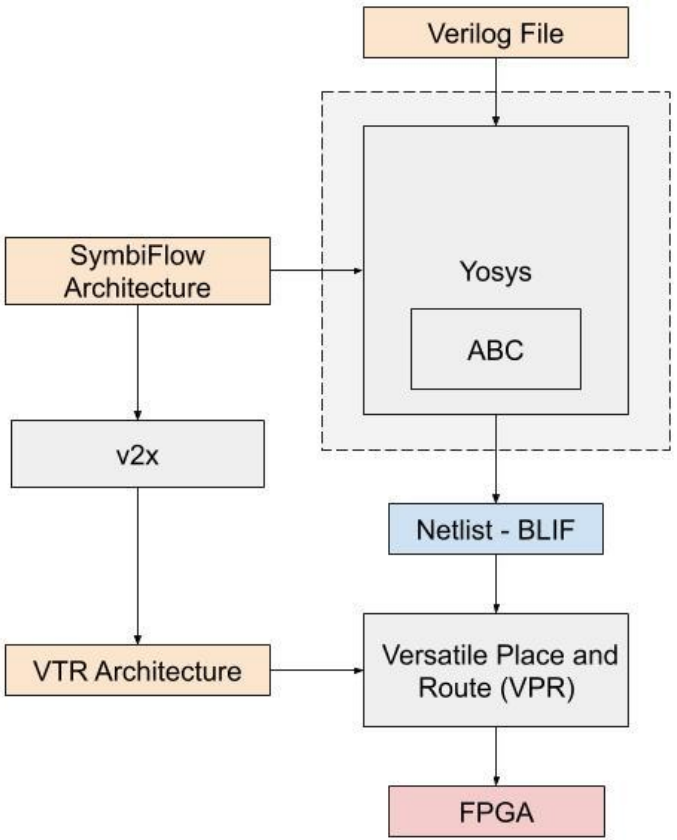
Verilog To Routing (VTR)

- Computer Aided Design (CAD) flow for FPGAs
- Open Source
- Written in C/C++



SymbiFlow

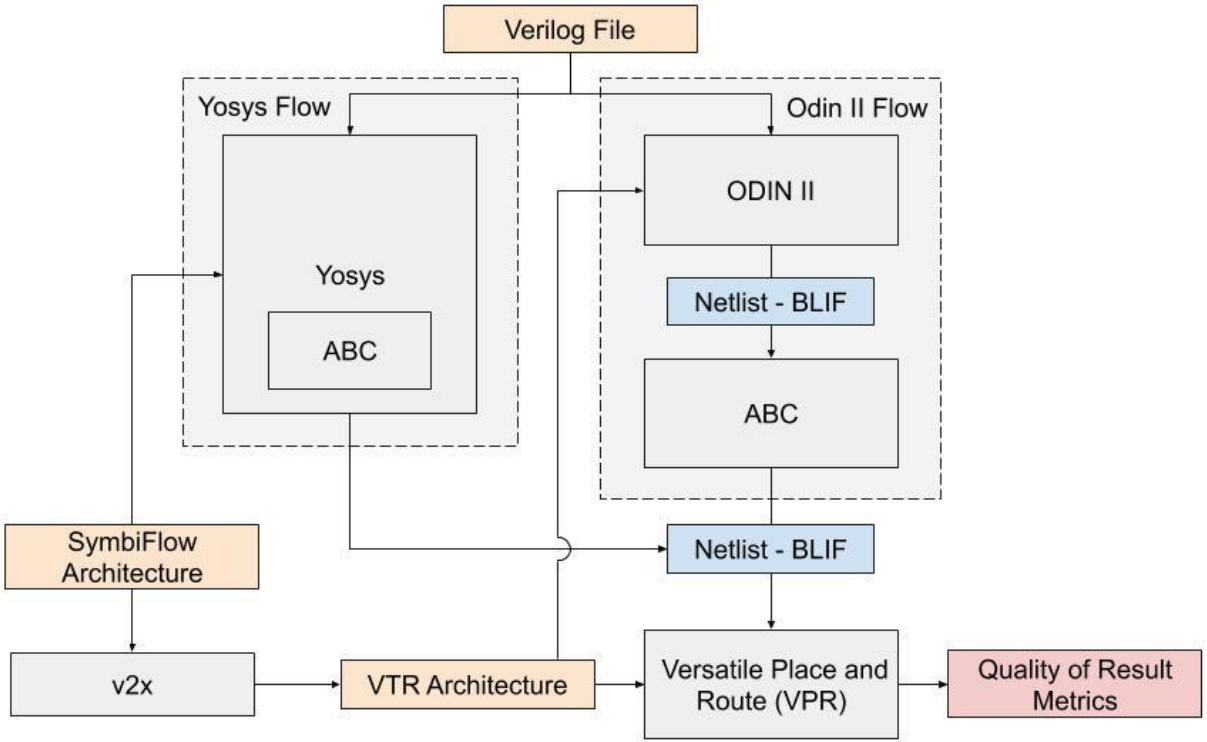
- Open Source project targeting commercial FPGAs
- Uses Yosys and VPR



Experiment Outcomes

- Produce a framework for future comparison
  - Against different architectures
  - Against different benchmarks
- Compare Quality of Result (QoR) of both tools
- Compare runtime characteristics of both tools

Full Benchmark Flow



Benchmark Methodology

- Select a range of compatible benchmarks
- Run each benchmark through both tools
  - This was repeated when gathering runtime statistics
- Run through VPR 10 times
  - VPR placement is non deterministic
- Gather QoR metrics output by VPR
  - Critical path delay, Logic area used
- Gather runtime metrics for each stage
  - Max. Resident Set Size (RSS), Total runtime

Artix-7 XC7A200T Architecture

- Popular line of FPGAs
- Provides benchmarks with real world basis
- Large enough for all benchmarks to place androute
- SymbiFlow project has built a VPR architecture description

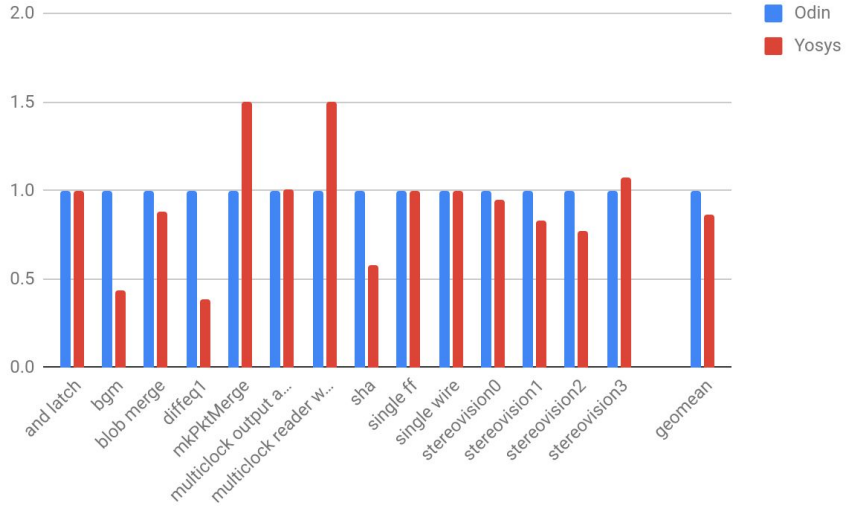
Benchmarks

- Benchmark from VTR's benchmark suite
- Supported by Odin-II
- Cover a wide range of real world uses
- Variety of sizes

Benchmark	Domain
and latch	Trivial
bgm	Finance
blob merge	Image Processing
diffeq1	Math
diffeq2	Math
mkPktMerge	Packet Processing
multiclock output and latch	Trivial
multiclock reader writer	Trivial
sha	Cryptography
single ff	Trivial
single wire	Trivial
stereovision0	Computer Vision
stereovision1	Computer Vision
stereovision2	Computer Vision
stereovision3	Computer Vision

Results - Critical Path Delay

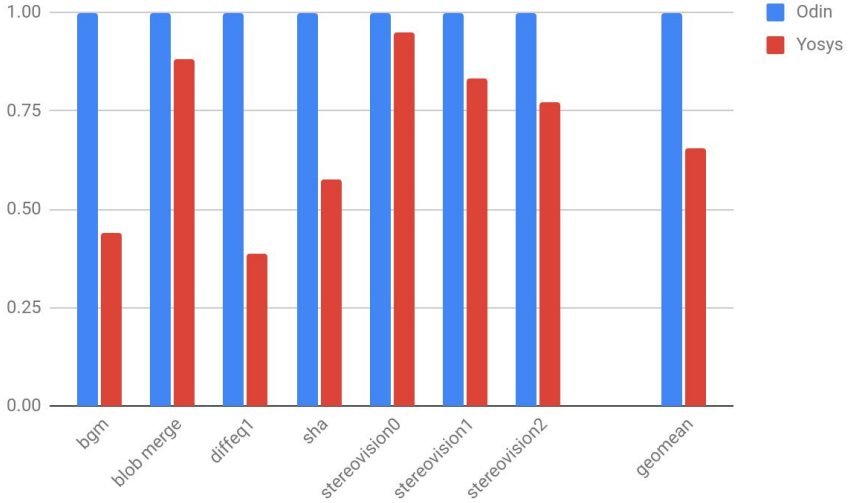
- Determines the maximum clock frequency
- Yosys geomean 86% of Odin-II



Normalised critical path delay of Odin-II vs Yosys flow

Results - Critical Path Delay >1000 blocks

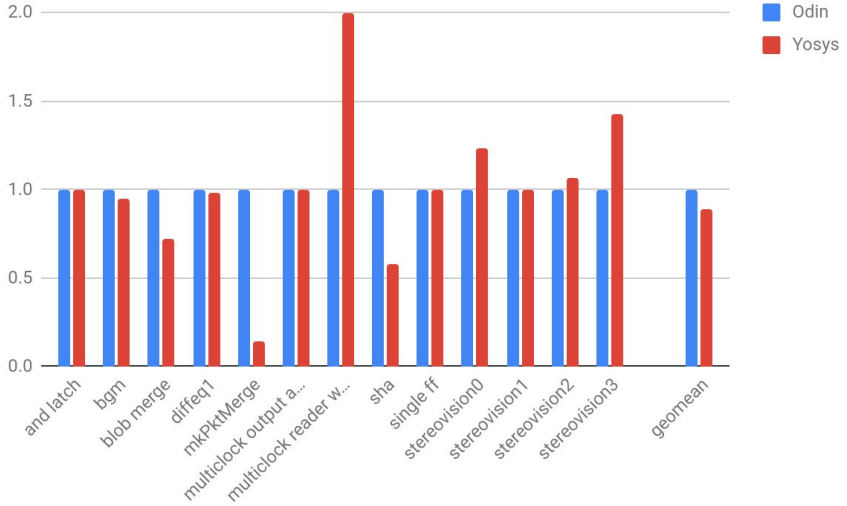
- Only benchmarks with >1000 blocks when synthesized with Odin-II
- Yosys geomean 66% of Odin-II



Normalised critical path delay of Odin-II vs Yosys flow for benchmarks with >1000 blocks

Results - Logic Area Used

- Influences the minimum size FPGA
- Influences power consumption
- Yosys geomean 89% of Odin-II



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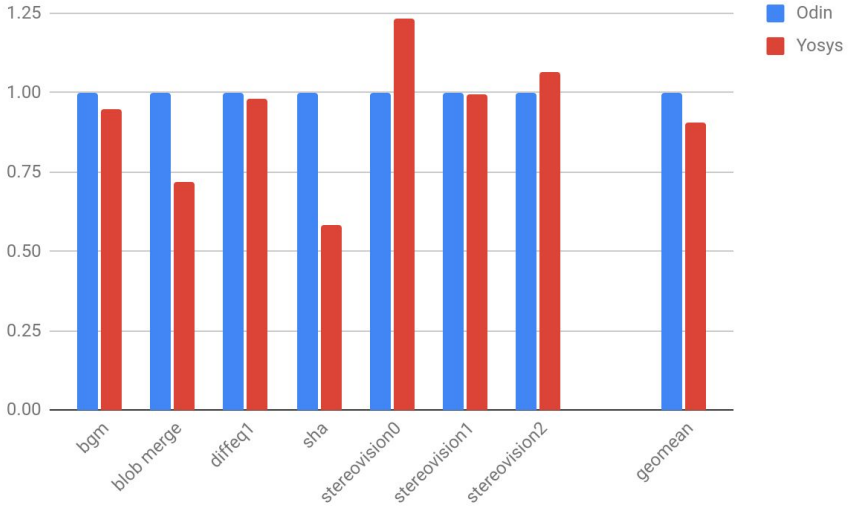
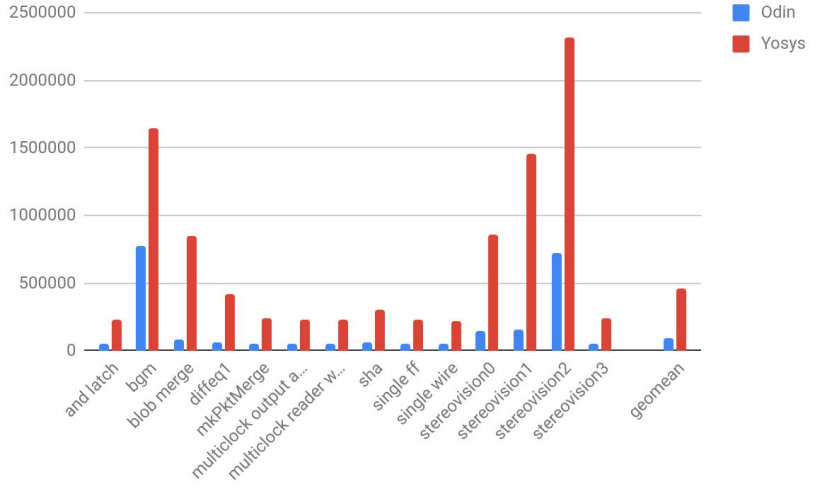


Normalised logic area used for Odin-II vs Yosys flow for benchmarks with >1000 blocks

Results - Synthesis Memory Consumption

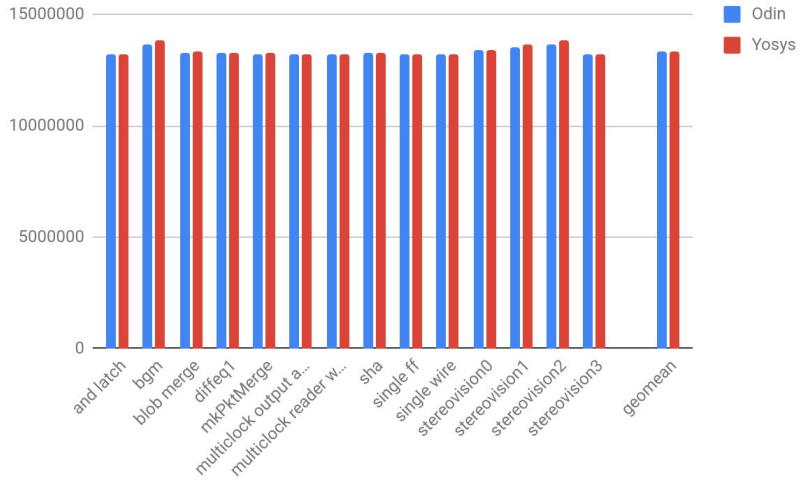
- Measures Maximum Resident Set Size (RSS)
- Includes ABC, but not VPR
- Yosys geomean 510% of Odin-II
- Relevant for
  - Small architectures
  - Verilog synthesis research
  - Circuit simulation



Max. RSS (KiB) for Odin-II vs Yosys synthesis

Results - VPR Memory Consumption

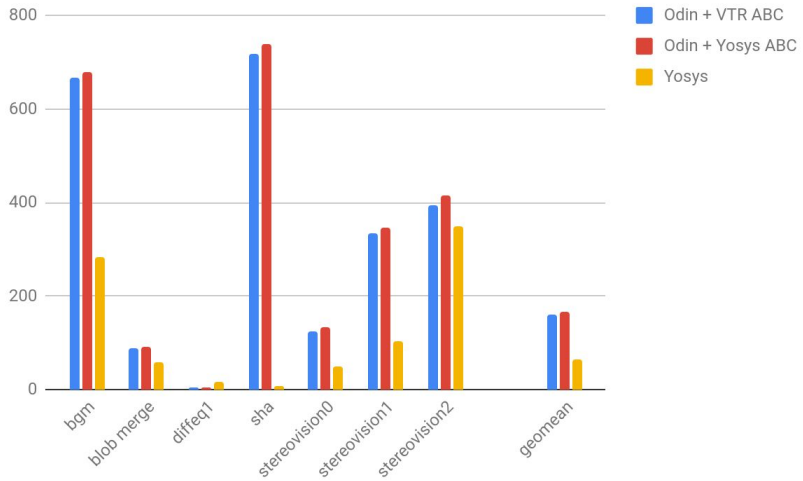
- Measures max. RSS
- Only includes VPR
- Much larger than max. RSS for synthesis step
- Dominated by architecture size
  - For smaller architectures synthesis may dominate



Max. RSS (KiB) of VPR in Odin-II flow vs Yosys flow

Results - Synthesis Run Time

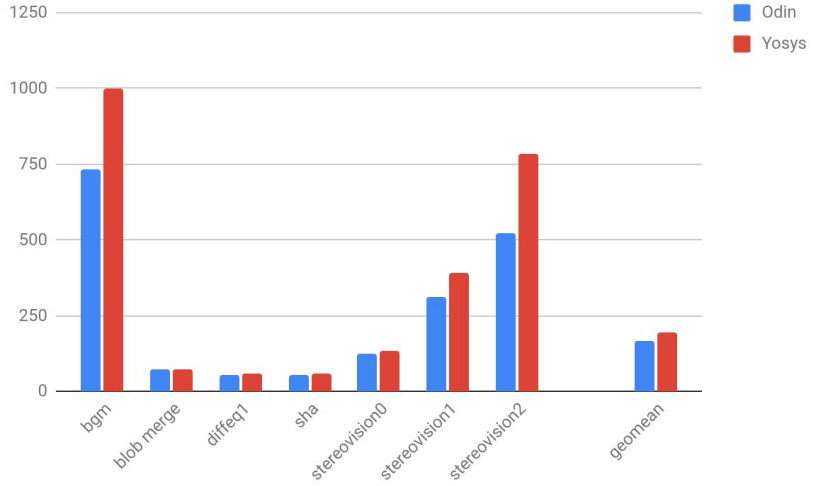
- Total run time of synthesis
- Only benchmarks >1000 blocks
  - Otherwise launch overheads dominate
- Includes ABC, but not VPR
- Yosys geomean 40% of Odin-II



Total runtime for Odin-II vs Yosys synthesis

Results - VPR Run Time

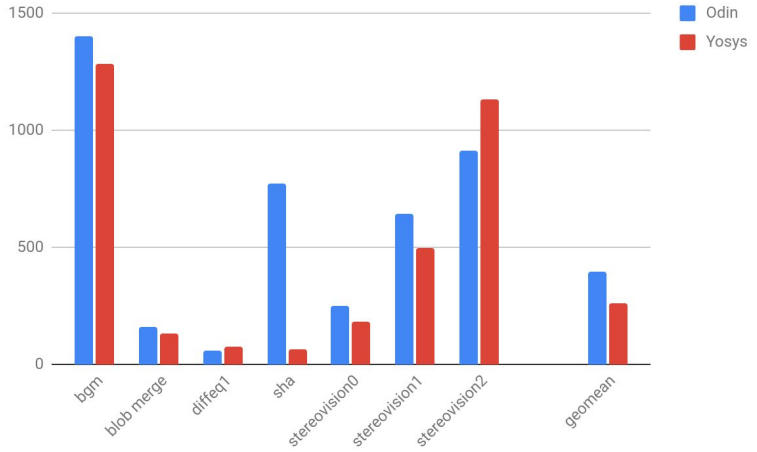
- Total run time of VPR
- Only includes VPR
- Only benchmarks >1000 blocks
- Yosys geomean 119% of Odin-II



Total run time of VPR in Odin-II flow vs Yosys flow

Results - Total Flow Run Time

- Total run time for entire flow
- Only benchmarks >1000 blocks
- Synthesis + VPR time
- Yosys geomean 67% of Odin-II



Combined runtime for full Odin-II vs Yosys flow

Limitations

- Yosys has been tuned against the Artix-7 family used in this comparison
- Technology mapping was disabled for this comparison
  - This ensured a fair comparison as Odin-II did not recognise the hard-blocks in the XC7A200T architecture
  - An important feature for real use cases
- The benchmarks used come from Odin-II's benchmark suite

Future Work

- Compare a broader range of architectures
- Compare a broader range of benchmarks
  - This may require improvement to Odin-II's language coverage
  - Titan Benchmark suite is a modern candidate
- Add hard-block support for Artix-7 family to Odin-II
  - Revisit this comparison with technology mapping enabled

Conclusion

- How do Odin-II and Yosys compare?
- Produced a framework to compare synthesis flows
  - Supports different architectures
  - Supports different benchmarks
- Gathered QoR and run time metrics for both tools
- Yosys tends to outperform Odin-II in most applications
  - Better in most run time and QoR metrics
- Odin-II synergises well with VPR out of the box