

## **Masaru Takesue**



Masaru Takesue received the Master degree in electronics in 1968 and the Doctor degree in engineering in 1990 both from the University of Kyushu, Japan. He joined with Nippon Telegraph and Telephone Public Corporation (now, NTT Communications) in 1968, and was engaged in the research on computer systems, including file systems, database machines, sequential and parallel computers, dataflow machines, and parallel and distributed algorithms. He moved to Hosei University, Tokyo, Japan in 1993, and is currently a professor, Department of Applied Informatics, Faculty of Science and Engineering. His current interest includes the security on computer and network systems, ILP microarchitectures in sequential computers, parallel computer architectures for several embedded applications such as image processing and IP packet routing, and sensor networks.

He has published many research papers, especially on the execution control and resource management of dataflow machines (IEEE ISCA, IEEE Trans. on Computers, ACM FJCC, IEICE Trans. on Computer Systems, IEICE JSPP), unification of cache coherence and synchronization for multiprocessors (ICPP, IEEE I-SPAN, EuroPal, IEICE Trans. on Computer Systems, IEICE JSPP), small diameter interconnection topologies for multiprocessors (ICPP, IEICE JSPP), and so on. Currently published papers are mainly on security; protection against information leakage from portable devices (IARIA SECURWARE), protocols for secure transfer of confidential data (IARIA SECURWARE, IEEE NAS), and personalized spam filtering (IARIA SECURWARE).

The goal of his research is a secure and portable supercomputer, integrating his research achievements in the areas of multiprocessors, embedded processors, and security schemes into a System-On Chip (SoC).

He is a member of IEEE, IEICE Japan, Editorial Board of IEICE Technical Committee on Computer Systems, and Editorial Board of IARIA International Journal on Advances in Security.

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