Integrated Sensor System for Signal Conditioning, Digitization and Interfacing for Terahertz Bolometric Camera

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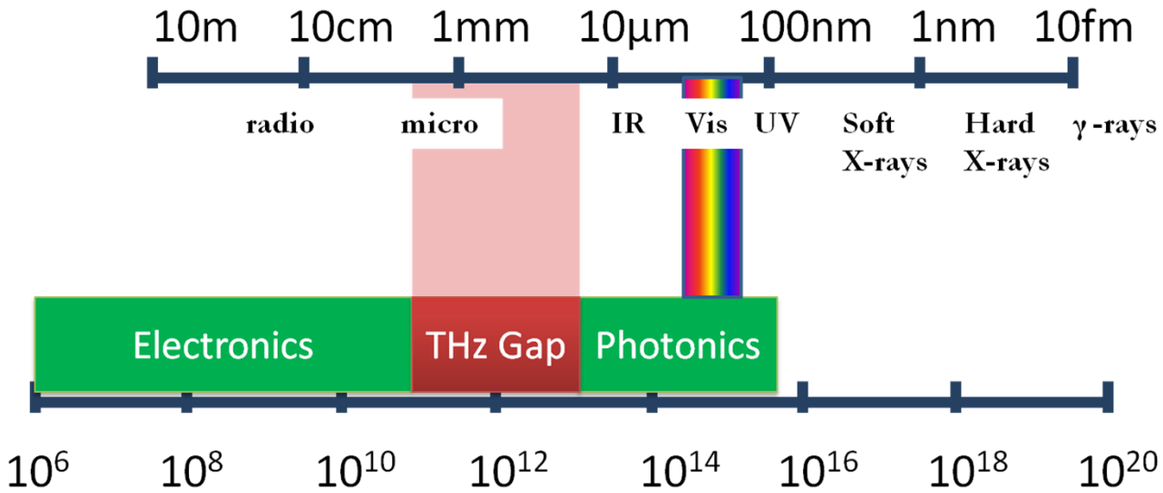
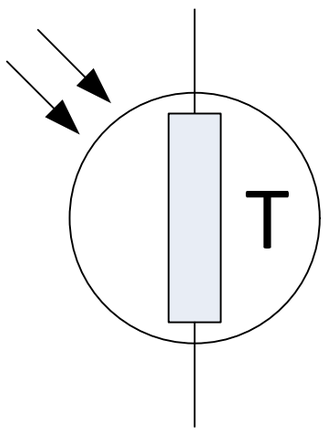
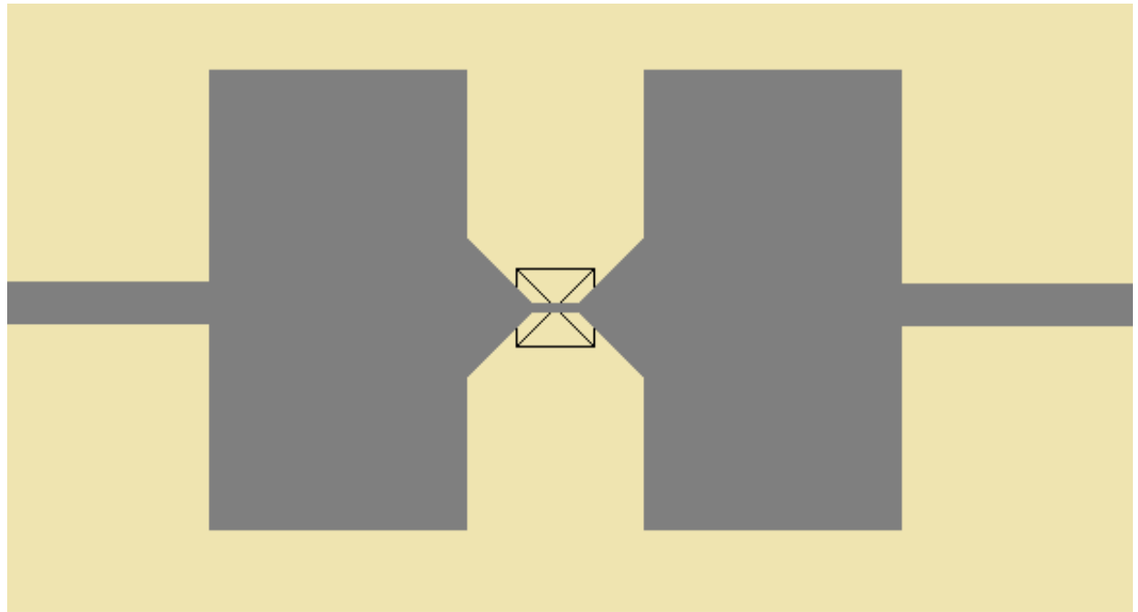
Agenda

- Introduction to THz and bolometers
- Idea
  - Existing system
  - Novel system
- Analogue processing
- Low-noise amplifier design
  - Lateral Bipolar Transistor Structure
- Conclusion

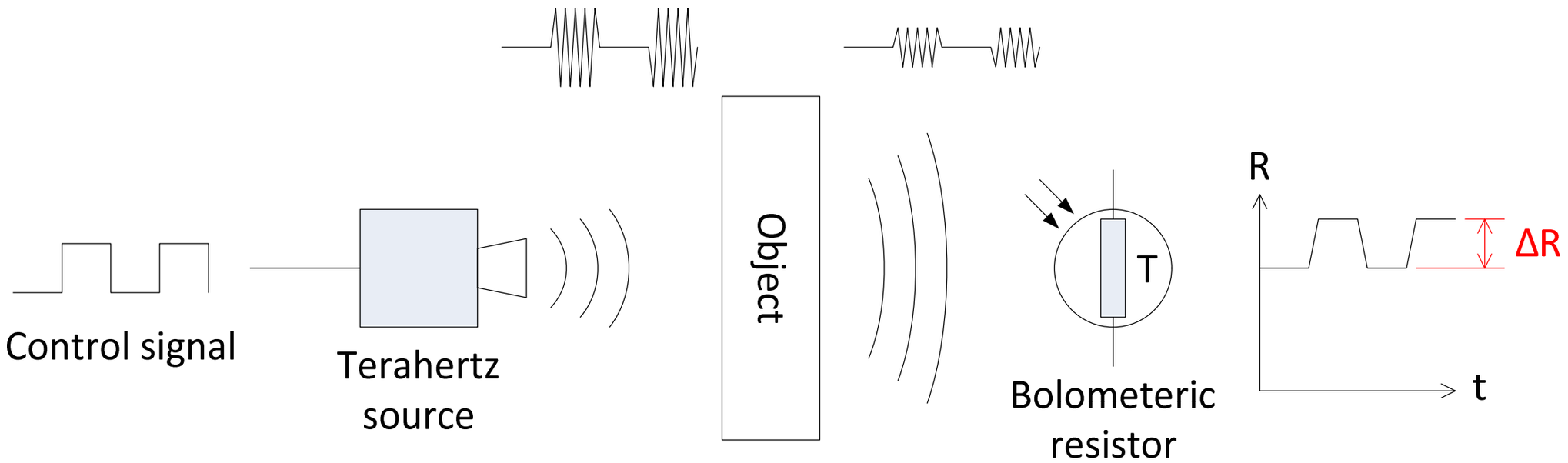
THz waves and Bolometers



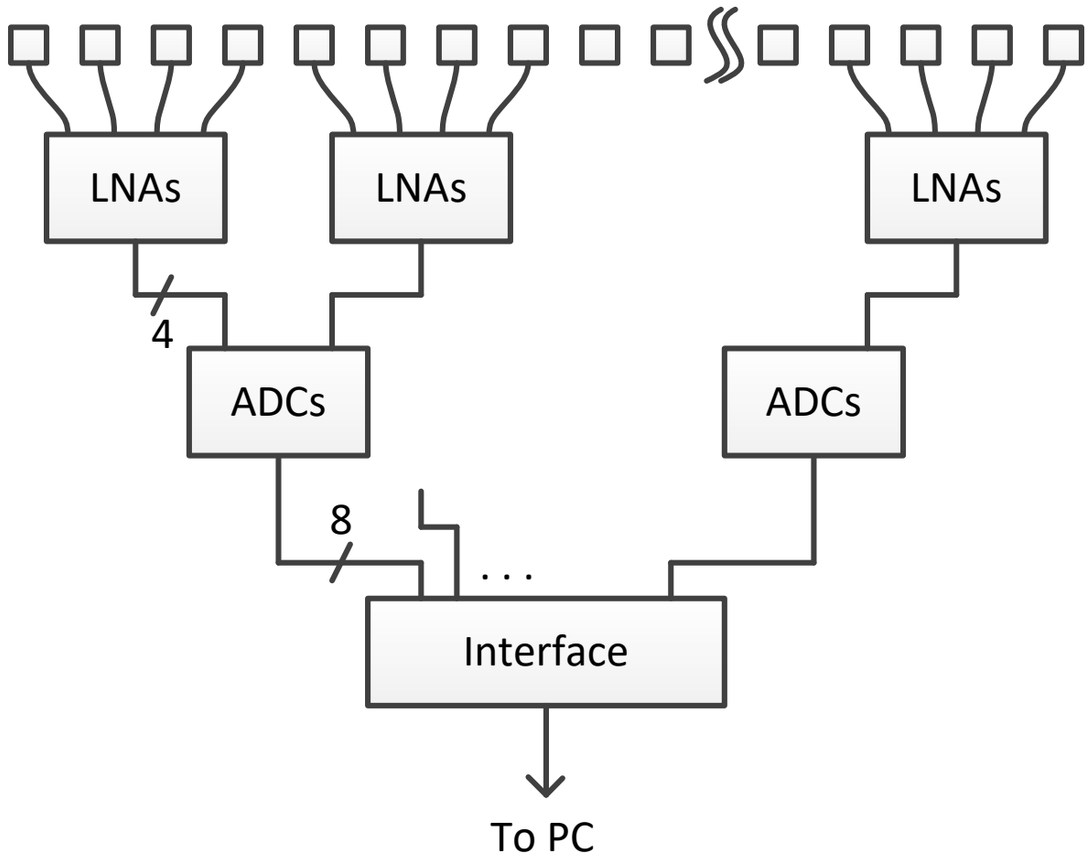




THz waves and Bolometers



Existing THz camera system



Bolometers

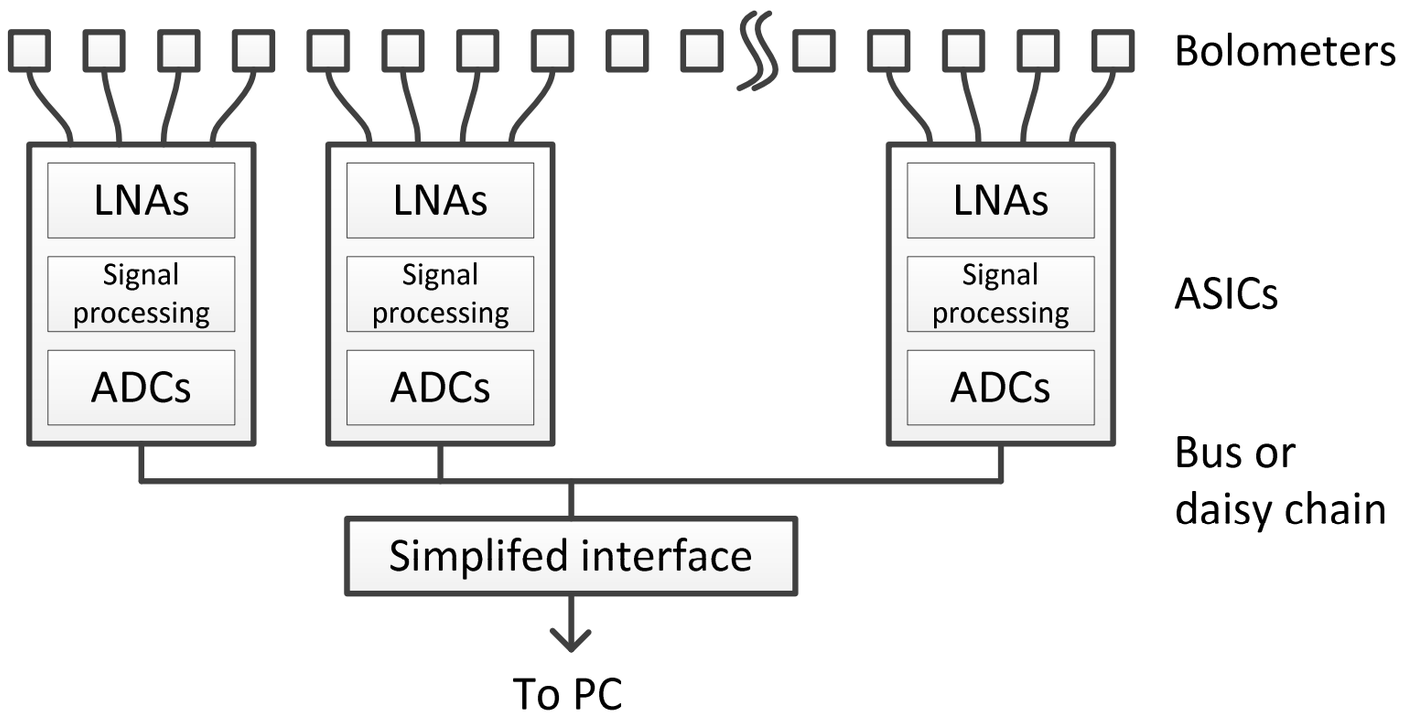
ASICs with low-noise amplifiers

16-bit 8-channel SAR ADCs

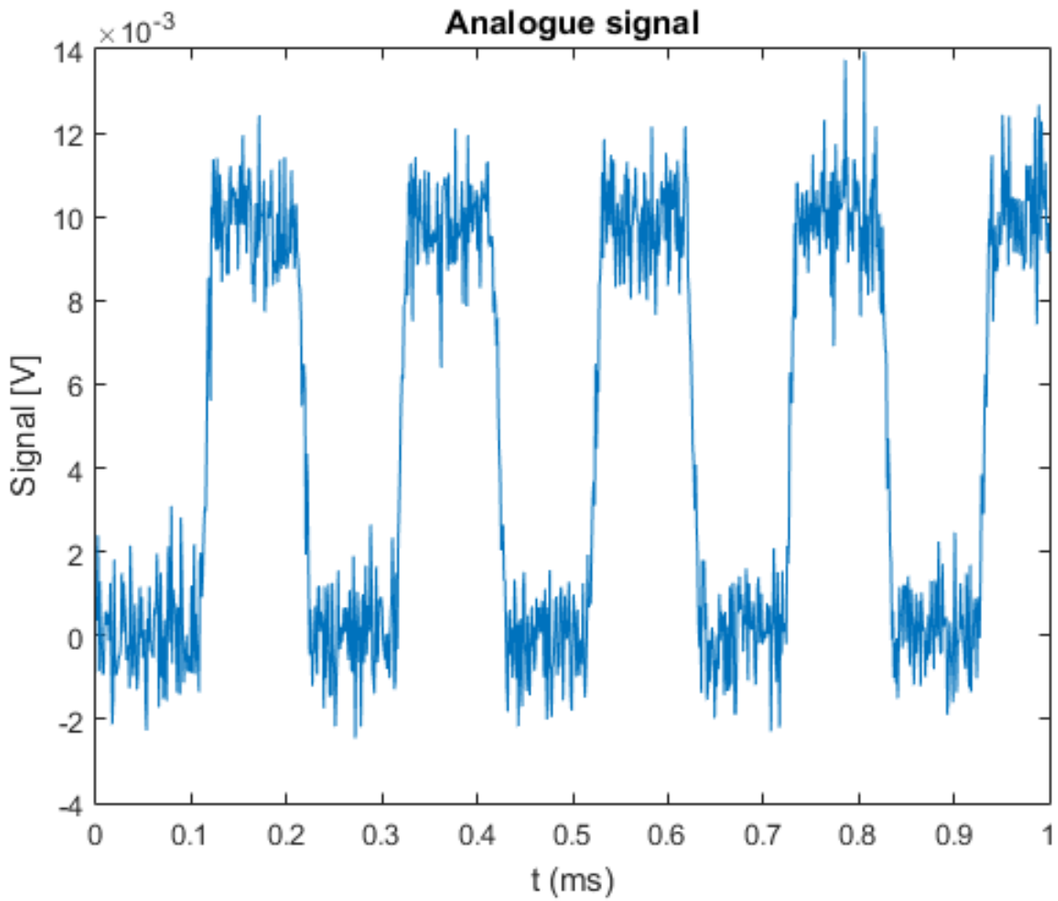
Powerful FPGA

Ethernet

Novel system



Noise rejection



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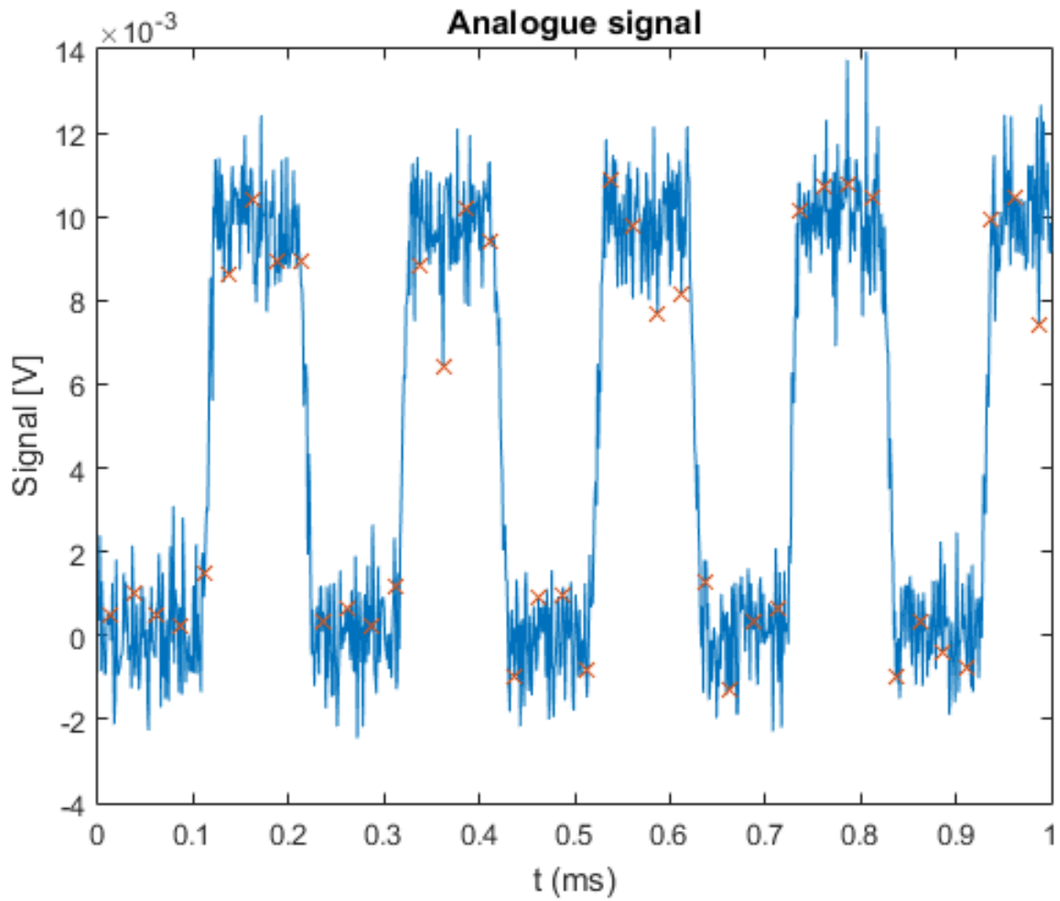

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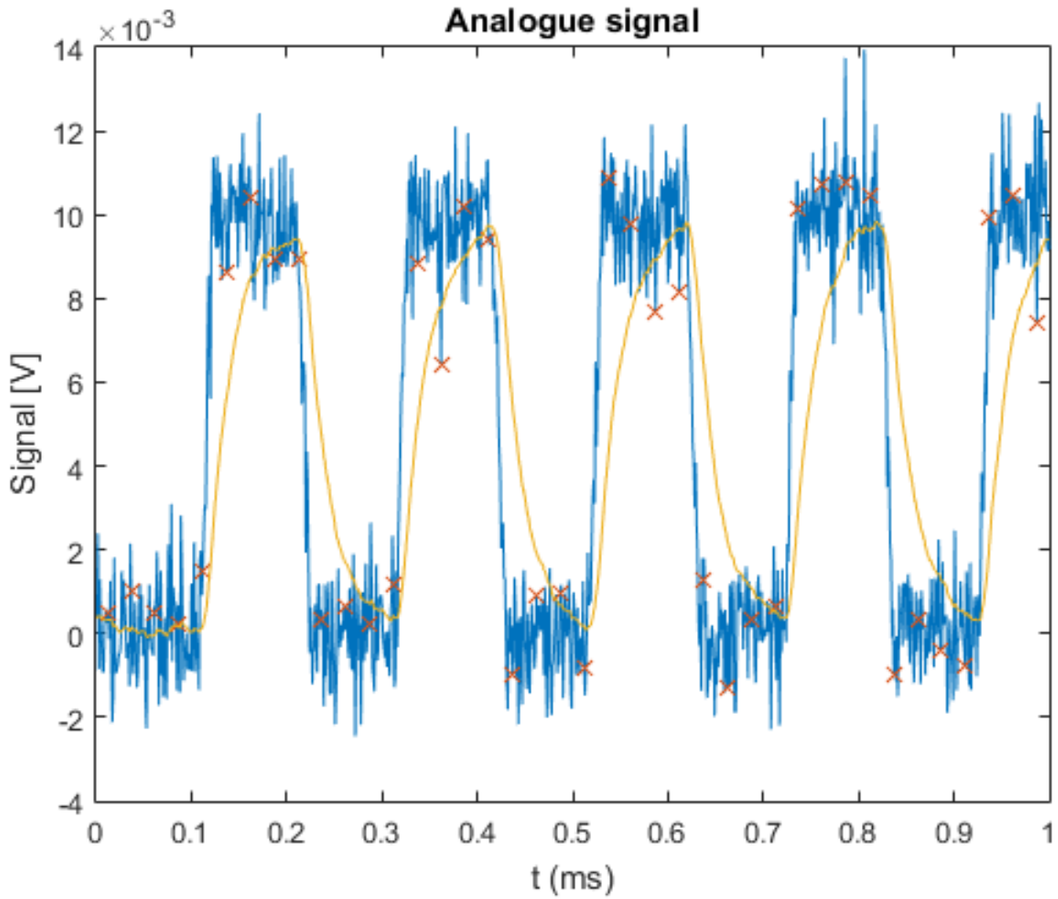
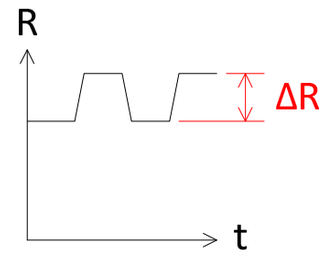
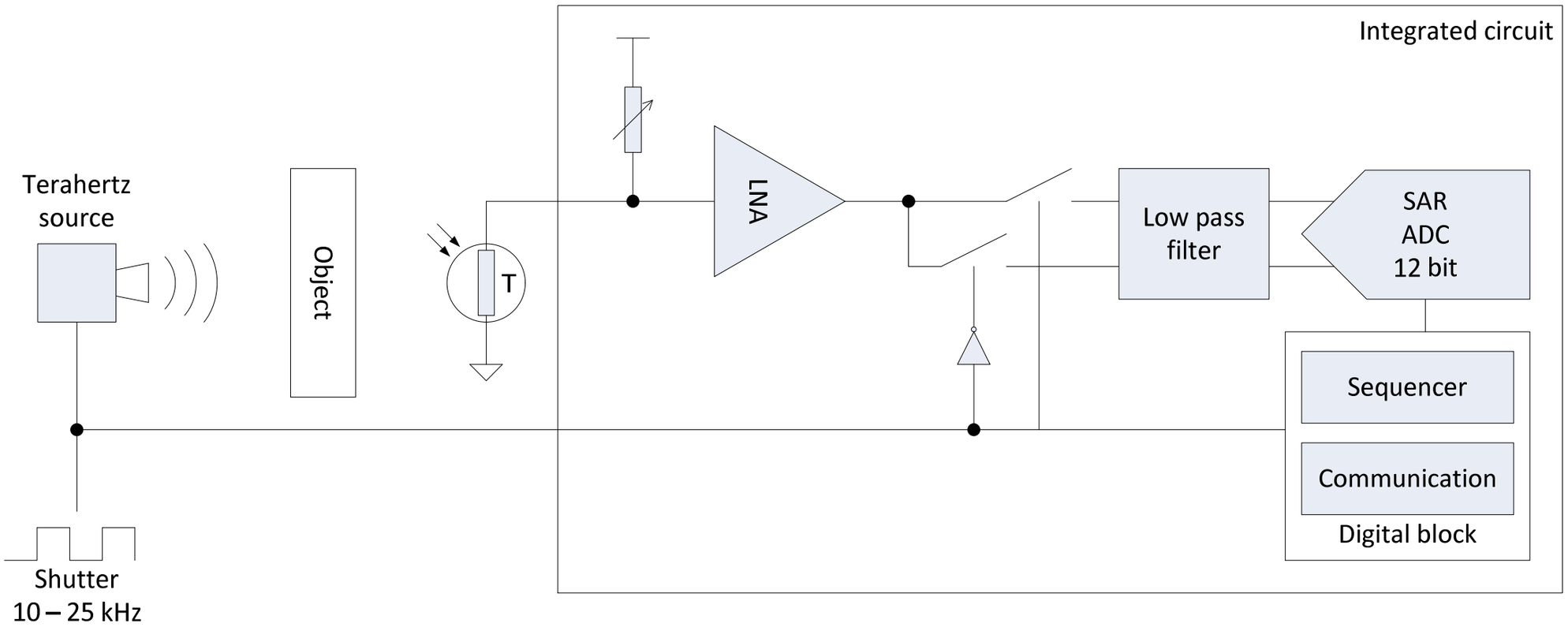


The integrated circuit





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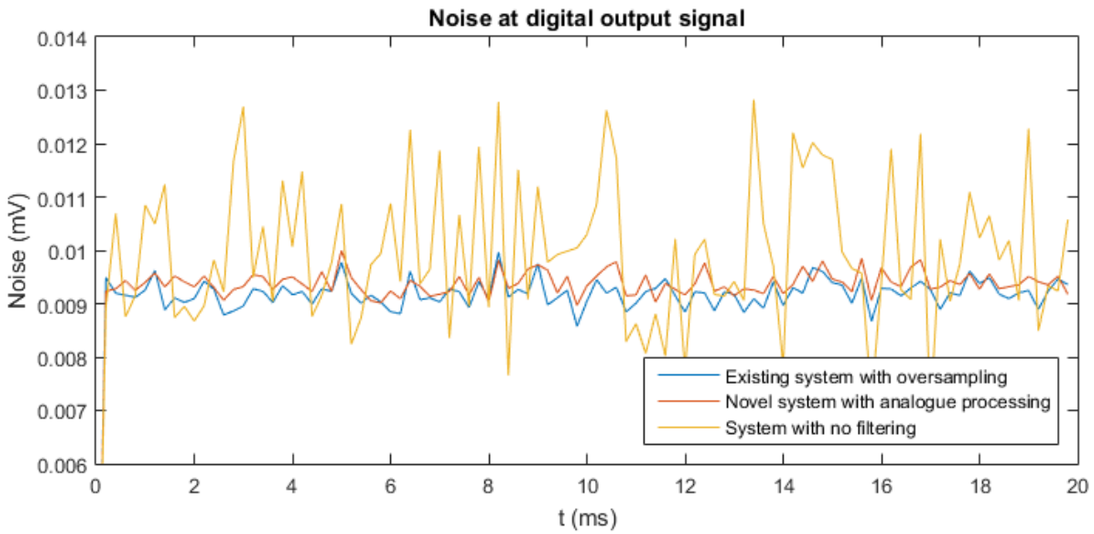
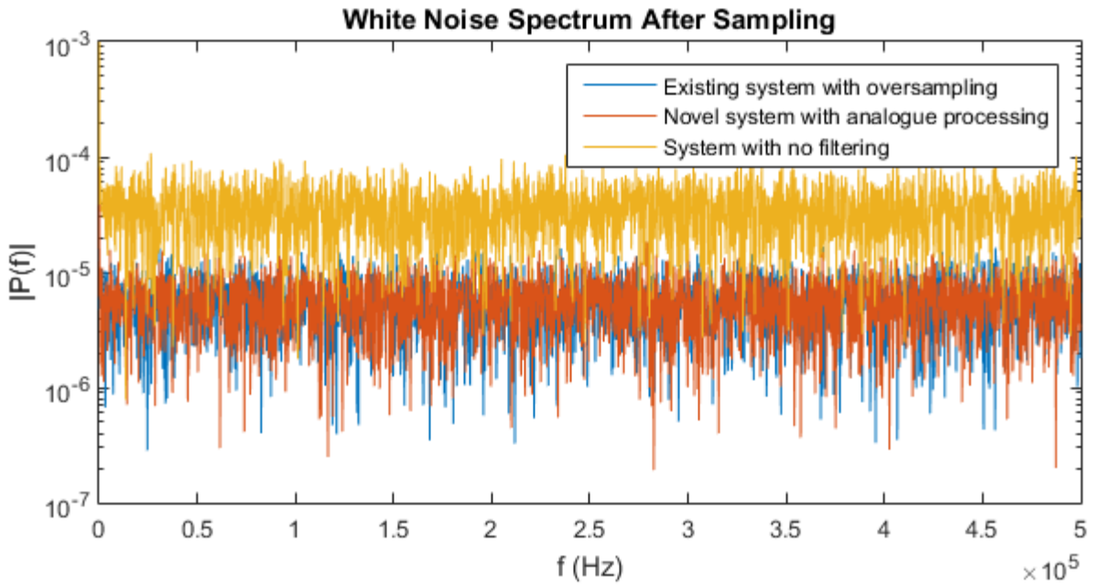


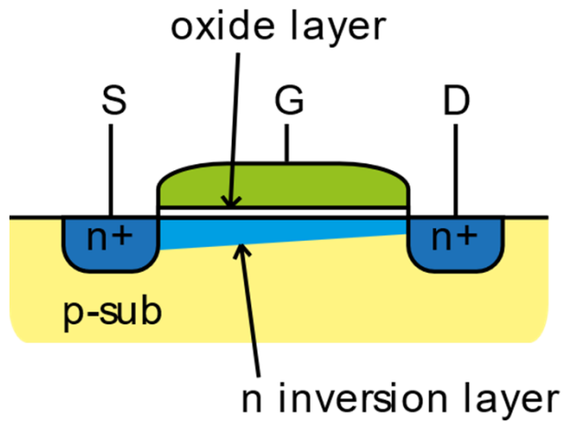


Amplifier

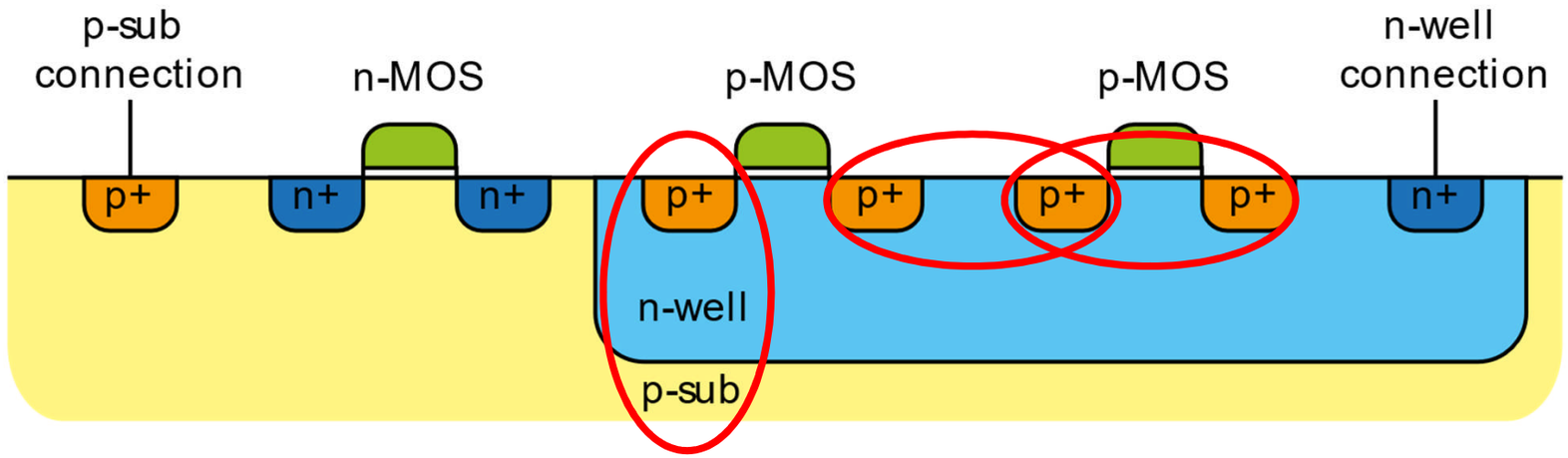
- Low noise amplifier (LNA) design
- Existing amplifier in Complementary metal-oxide-semiconductor (CMOS) technology
  - 5nV/√Hz noise at 1kHz
  - 60dB closed loop gain
  - ~900uA current consumption
  - ~0.5mm^2 area
- Requirement for new amplifier
  - 2nV/√Hz
  - Same gain
  - Power consumption not increased
  - Area not increased
  - Same technology (CMOS 0.35um)

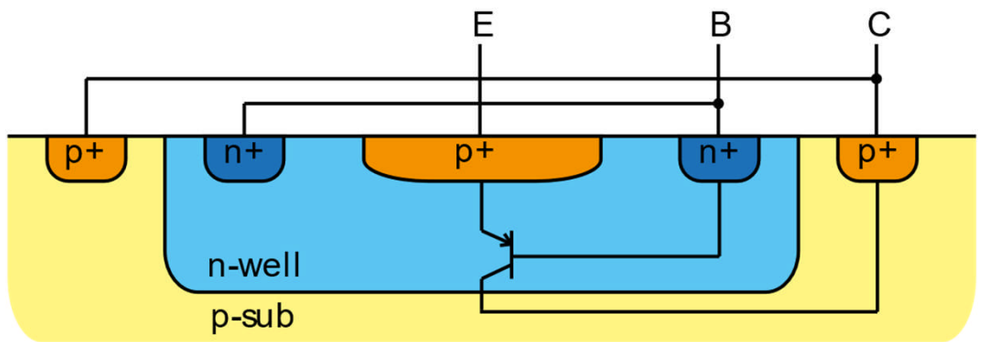
CMOS to BJT noise comparison

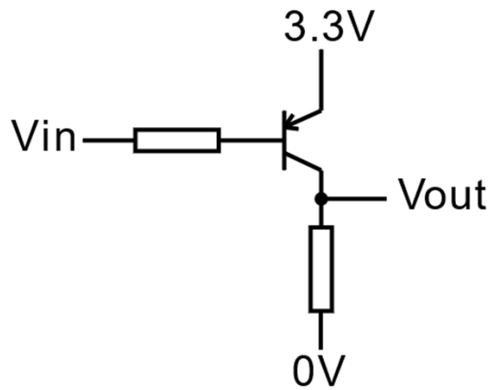
- (C)MOS Transistor
  - Charge carriers trapped in oxide layer
  - Scattering in inversion layer
  - 1/f dominant noise
- BJT (Bipolar Junction Transistor)
  - No inversion layer
  - White noise inversely proportional to collector current



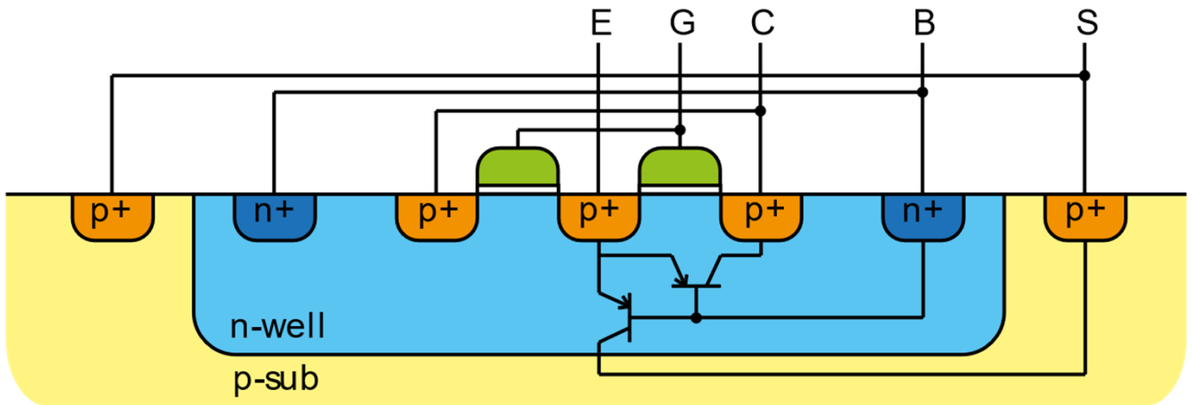
Layers in TSMC 0.35µm CMOS

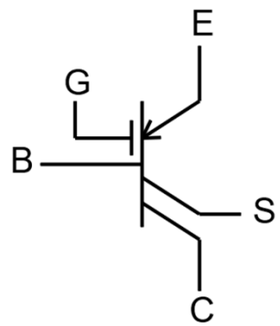






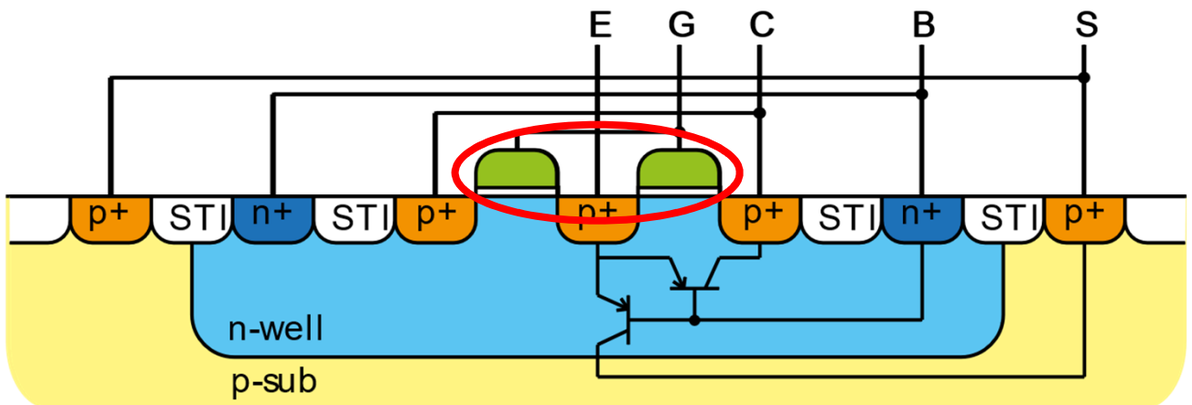
Lateral bipolar transistor structure

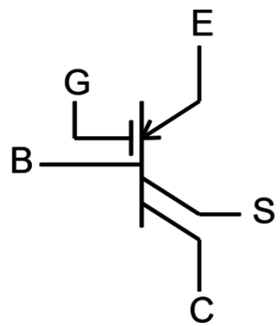




Purpose of the gate

- Shallow trench isolation (STI)





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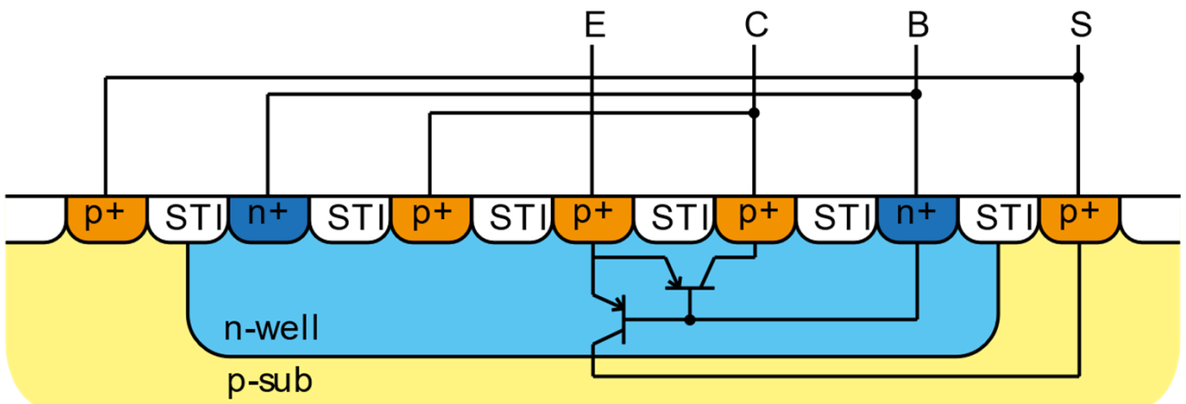
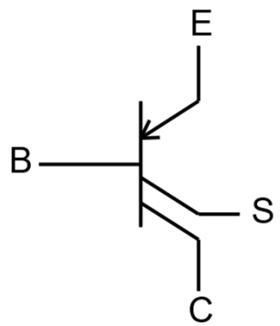
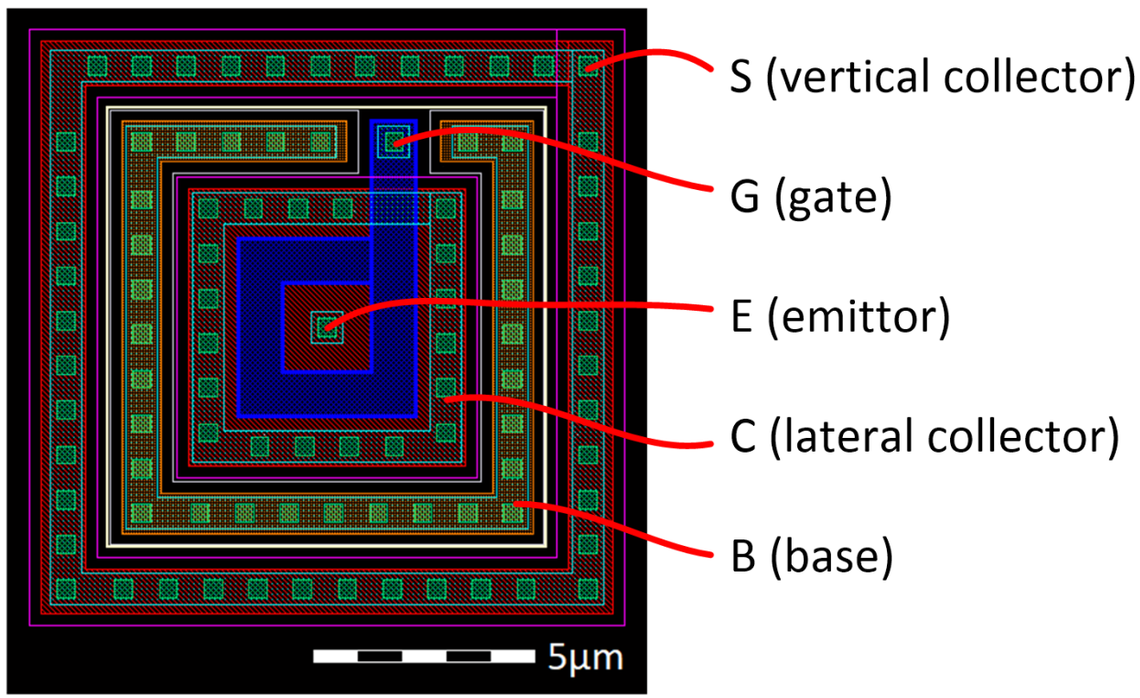




Test structures

- Initial design taken from a similar CMOS technology of a different fab
- Emitter size 2µm x 2µm
- Device size 13µm x 13µm (array pitch 11.5µm)
- Test structure is an array of 200 devices
- Two structures with different gate length

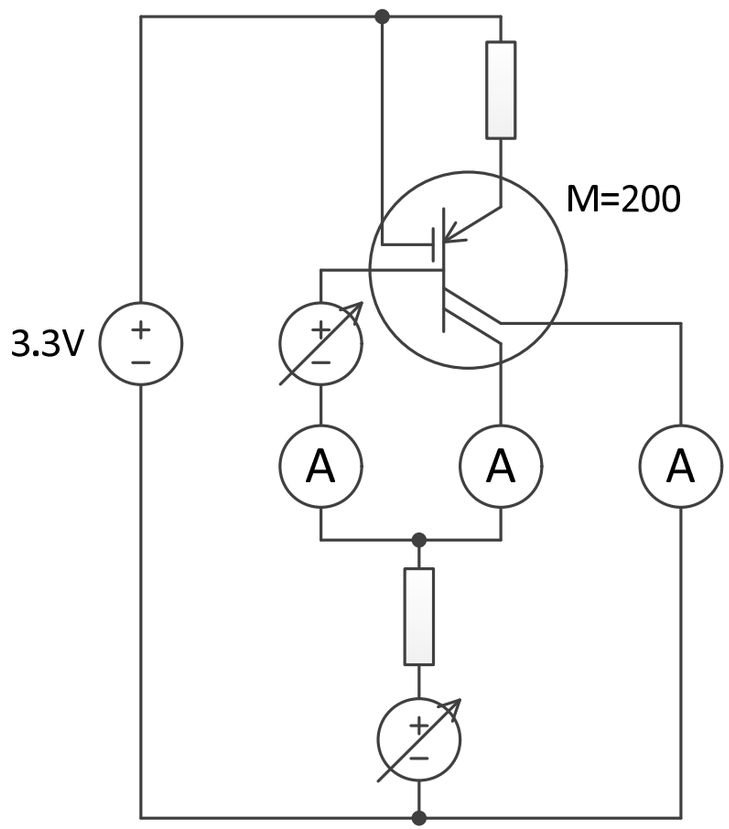


Test structures measurement

- Aim to determine β factors for both, lateral and vertical collector

  $\beta = I_C / I_B$

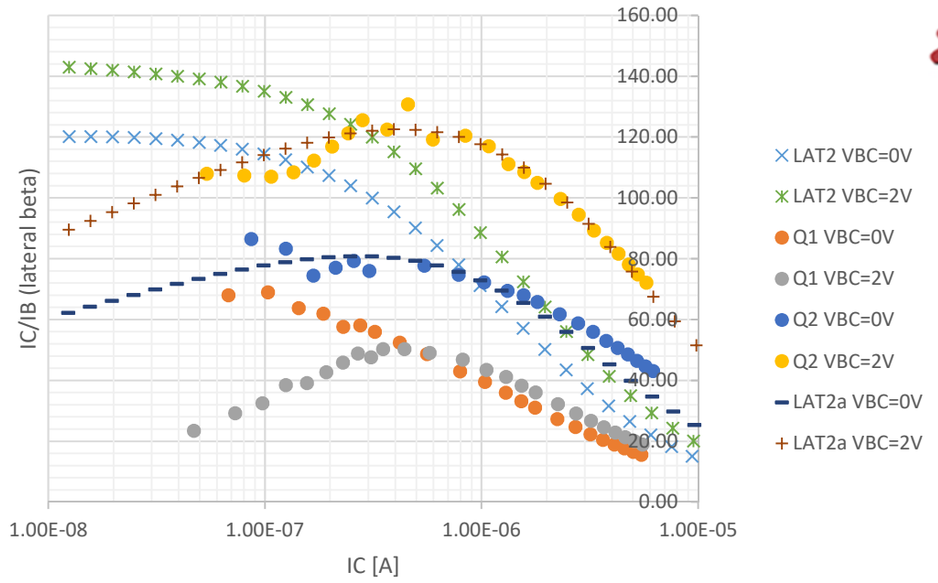
- Sweep collector current for different V_{BC} conditions

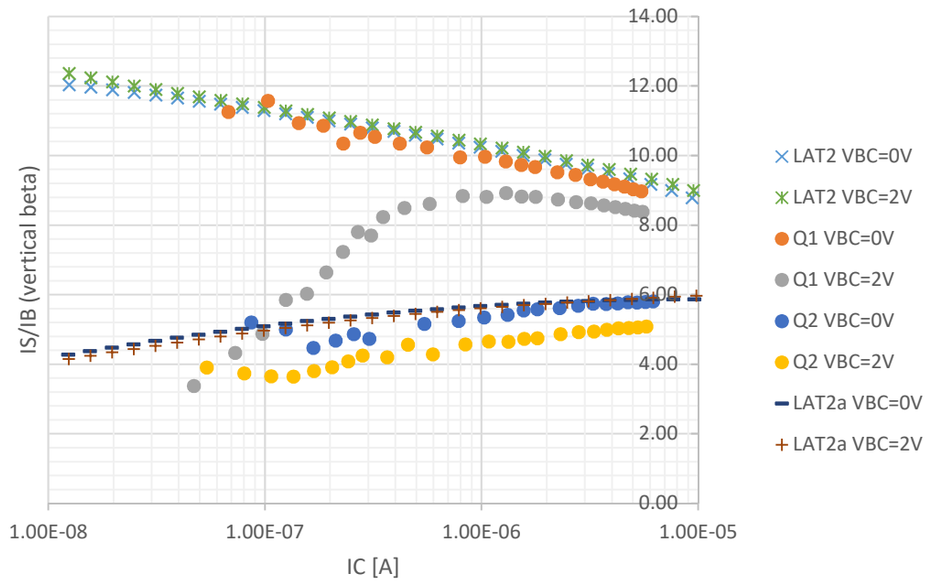


Results

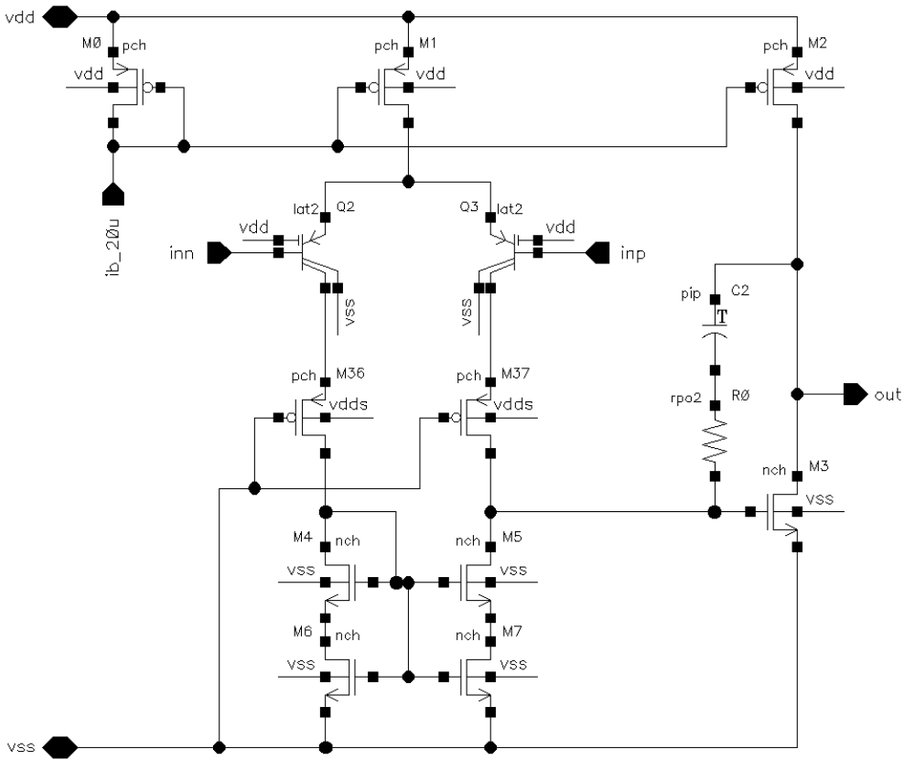
In comparison to LAT2 model

- Q1
  - Smaller β_{LAT}
  - Unaffected by V_{BC}
- Q2
  - Better β_{LAT} at higher currents
  - Smaller β_{VERT}





Amplifier design



Simulation results		
	Existing CMOS LNA	This work
I supply	948.5 µA	499.9 µA
Input noise at 100 Hz	12.86 nV/√Hz	5.062nV/√Hz
Input noise at 1 kHz	4.99 nV/√Hz	2.637nV/√Hz
Silicon area	0.516 mm^2	0.22 mm^2

Yet to be tested!

Conclusion

- Demonstrated feasibility of novel system
  - Analogue processing shows promising results
  - Reduced hardware cost
- New low-noise amplifier
  - Use of custom structures
  - Promising simulation results
- More work to be done

Thank you for your attention