Integrated Sensor System for Signal Conditioning, Digitization and Interfacing for Terahertz Bolometric Camera

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Agenda

• Introduction to THz and bolometers
• Idea
  • Existing system
  • Novel system
• Analogue processing
• Low-noise amplifier design
  • Lateral Bipolar Transistor Structure
• Conclusion
THz waves and Bolometers
THz waves and Bolometers
Existing THz camera system

- Bolometers
- ASICs with low-noise amplifiers
- 16-bit 8-channel SAR ADCs
- Powerful FPGA
- Ethernet

LNAs → ADCs → Interface → To PC
Novel system
Noise rejection
Noise rejection
Noise rejection

![Analogue signal graph]

- Signal [V]
- t (ms)
- $10^{-3}$

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The integrated circuit
Noise rejection

**Noise at digital output signal**

**White Noise Spectrum After Sampling**

- Existing system with oversampling
- Novel system with analogue processing
- System with no filtering
Amplifier

• Low noise amplifier (LNA) design
• Existing amplifier in Complementary metal-oxide-semiconductor (CMOS) technology
  • 5nV/√Hz noise at 1kHz
  • 60dB closed loop gain
  • ~900uA current consumption
  • ~0.5mm² area
• Requirement for new amplifier
  • 2nV/√Hz
  • Same gain
  • Power consumption not increased
  • Area not increased
  • Same technology (CMOS 0.35um)
CMOS to BJT noise comparison

- **(C)MOS Transistor**
  - Charge carriers trapped in oxide layer
  - Scattering in inversion layer
  - 1/f dominant noise

- **BJT** (Bipolar Junction Transistor)
  - No inversion layer
  - White noise inversely proportional to collector current
Layers in TSMC 0.35µm CMOS
Lateral bipolar transistor structure
Purpose of the gate

• Shallow trench isolation (STI)
Purpose of the gate

• Shallow trench isolation (STI)
Test structures

• Initial design taken from a similar CMOS technology of a different fab
• Emitter size $2\mu m \times 2\mu m$
• Device size $13\mu m \times 13\mu m$ (array pitch $11.5\mu m$)
• Test structure is an array of 200 devices
• Two structures with different gate length
Test structures measurement

- Aim to determine $\beta$ factors for both, lateral and vertical collector
  
  $\beta = \frac{I_C}{I_B}$

- Sweep collector current for different $V_{BC}$ conditions
Results

In comparison to LAT2 model

• Q1
  • Smaller $\beta_{\text{LAT}}$
  • Unaffected by $V_{\text{BC}}$

• Q2
  • Better $\beta_{\text{LAT}}$ at higher currents
  • Smaller $\beta_{\text{VERT}}$
Amplifier design

***Simulation results***

<table>
<thead>
<tr>
<th></th>
<th>Existing CMOS LNA</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>I supply</td>
<td>948.5 μA</td>
<td>499.9 μA</td>
</tr>
<tr>
<td>Input noise at 100 Hz</td>
<td>12.86 nV/√Hz</td>
<td>5.062 nV/√Hz</td>
</tr>
<tr>
<td>Input noise at 1 kHz</td>
<td>4.99 nV/√Hz</td>
<td>2.637 nV/√Hz</td>
</tr>
<tr>
<td>Silicon area</td>
<td>0.516 mm$^2$</td>
<td>0.22 mm$^2$</td>
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Yet to be tested!
Conclusion

• Demonstrated feasibility of novel system
  • Analogue processing shows promising results
  • Reduced hardware cost

• New low-noise amplifier
  • Use of custom structures
  • Promising simulation results

• More work to be done
Thank you for your attention