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COMPUTING WITH NANO-CROSSBAR ARRAYS

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Emerging Circuits and Computation (ECC) Group

Oct. 28th, 2019

The Twelfth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS'19)

Project Details

- Gathers globally leading research groups working on nanoelectronics and EDA
- Targets variety of emerging technologies including nanowire/nanotube crossbar arrays, magnetic switch-based structures, and crossbar memories
- Contributes to the construction of emerging computers beyond CMOS by proposing nano-crossbar based computer architectures.
- Budget: 724500 EURO

NANOxCOMP
Synthesis and Performance Optimization of a Switching Nano-Crossbar Computer

- **Dr. Mustafa Altun, – Coordinator** – Emerging Circuits and Computation Group, Istanbul Technical University, Turkey
- **Dr. Dan Alexandrescu**, IROC Technologies, Grenoble, France
- **Dr. Lorena Anghel**, TIMA Lab., Grenoble, France
- **Dr. Valentina Ciriani**, ALOS Lab., University of Milan, Italy.
- **Dr. Csaba A. Moritz**, Nanoscale Computing Fabrics Lab., University of Massachusetts, USA
- **Dr. Kaushik Roy**, Nanoelectronics Research Lab., Purdue University, USA
- **Dr. Georgios Sirakoulis**, Department of Electrical and Computer Engineering, Democritus University of Thrace, Greece
- **Dr. Mircea Stan**, High-Performance Low-Power Lab., University of Virginia, USA
- **Dr. Mehdi B. Tahoori**, Dependable Nano-Computing Group, Karlsruhe Institute of Technology, Germany

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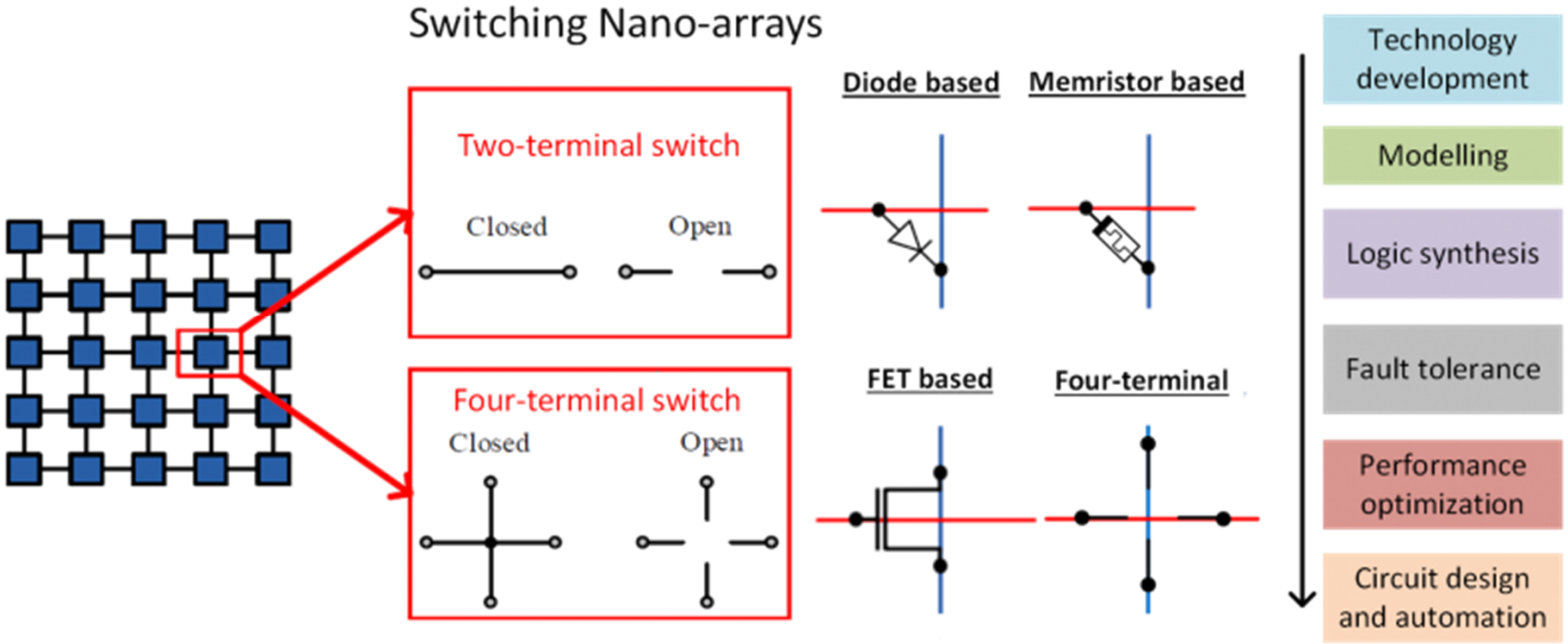
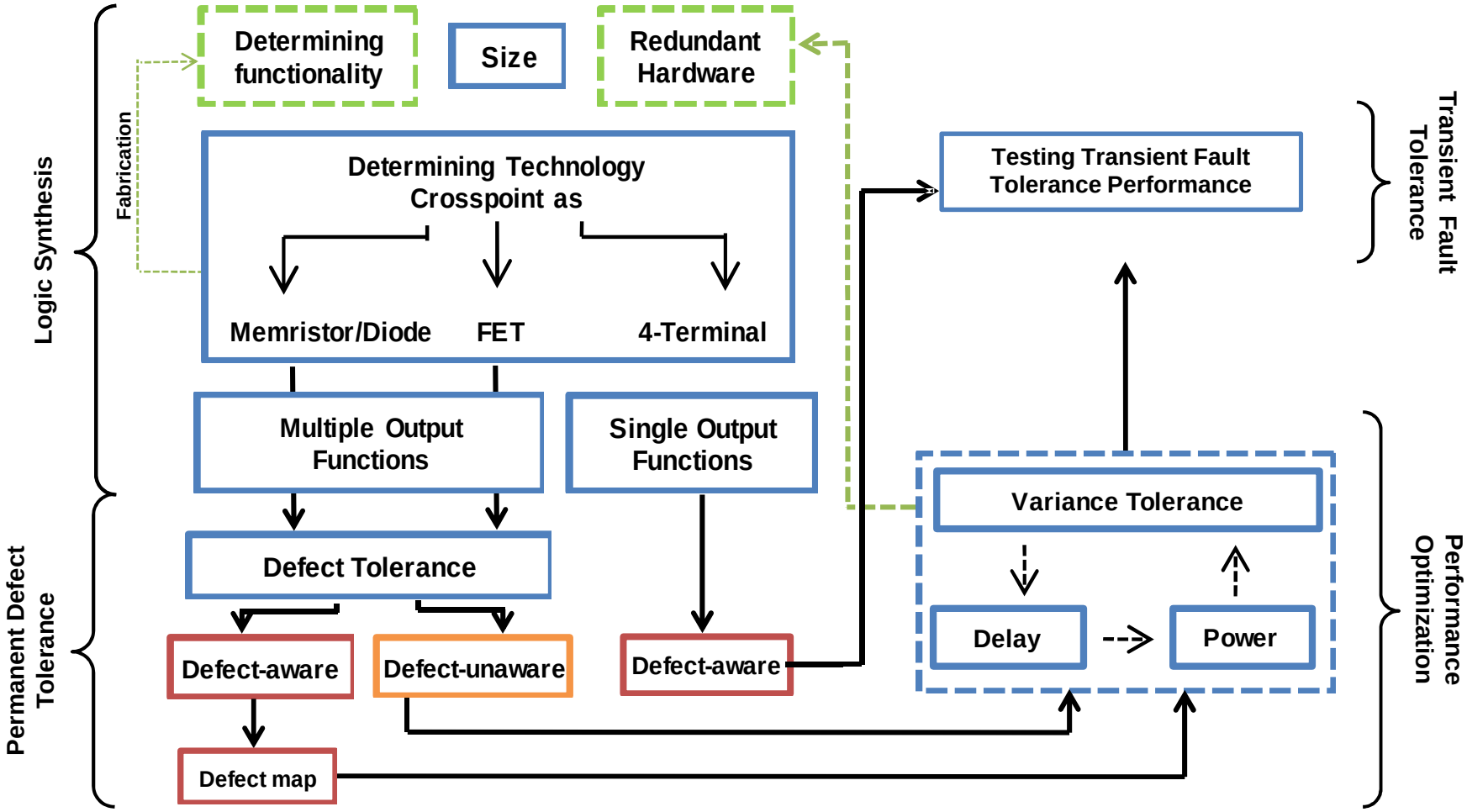
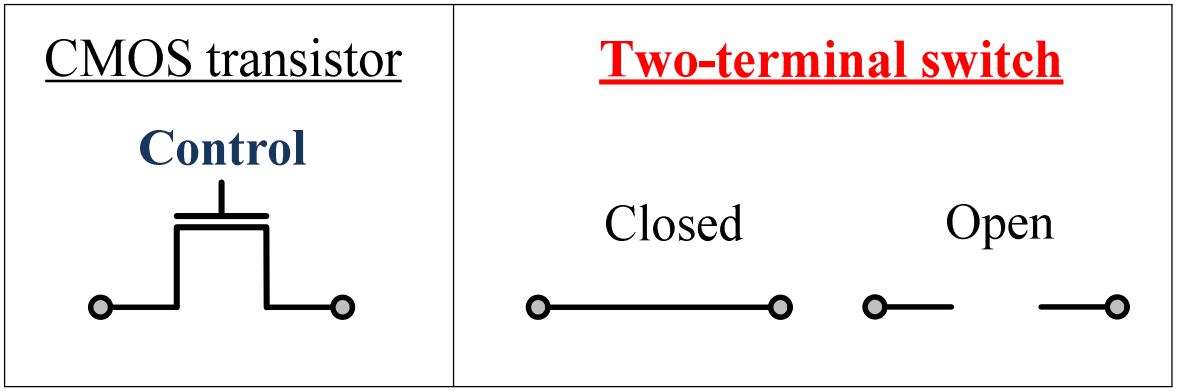
Project Details

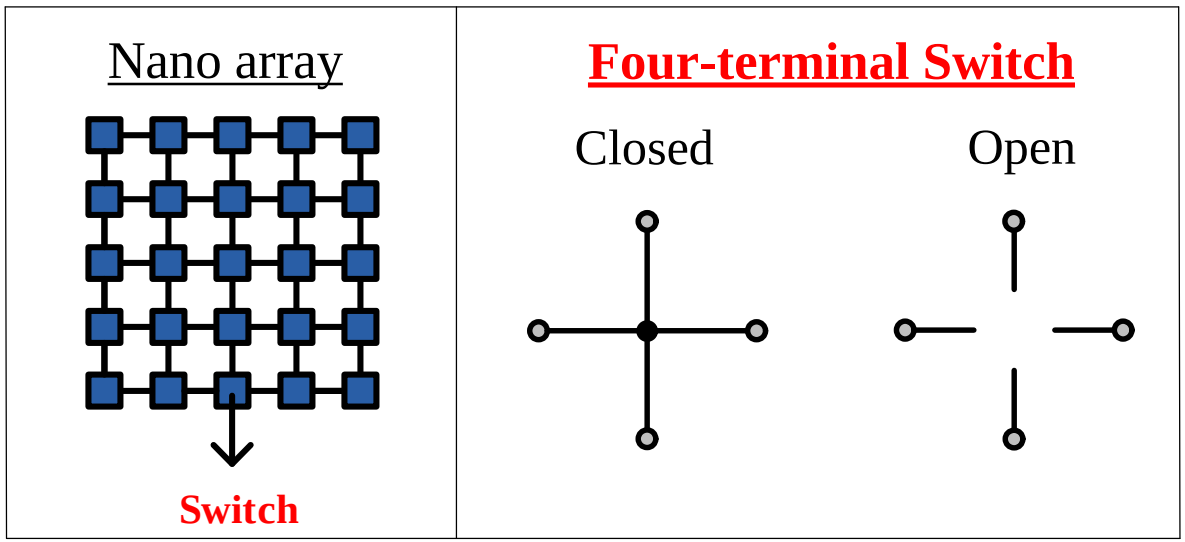


Project Details



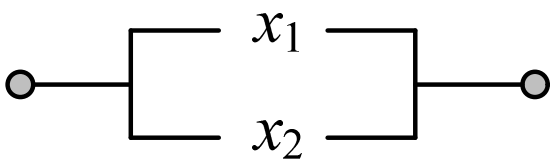
Two-terminal vs. Four-terminal



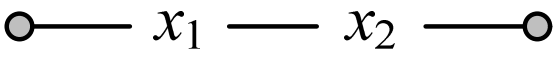


Two-terminal vs. Four-terminal

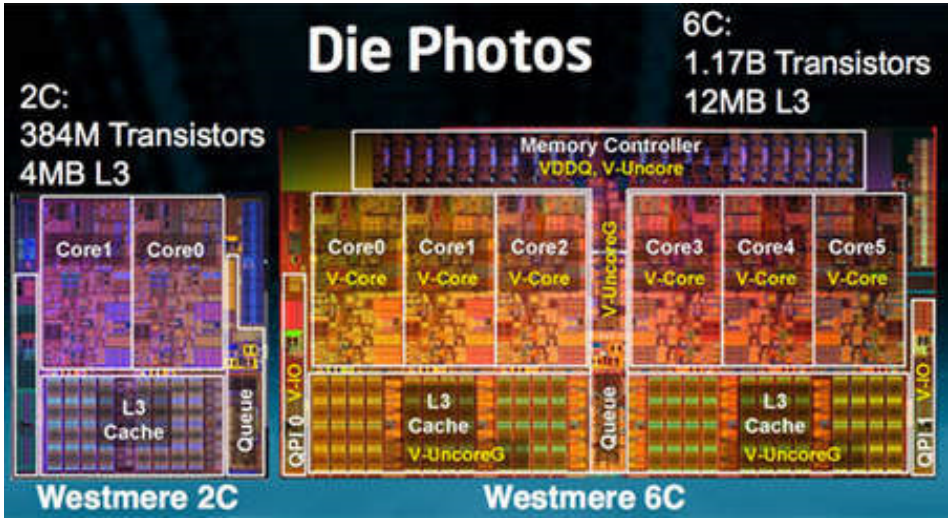
Shannon's work: *A Symbolic Analysis of Relay and Switching Circuits(1938)*



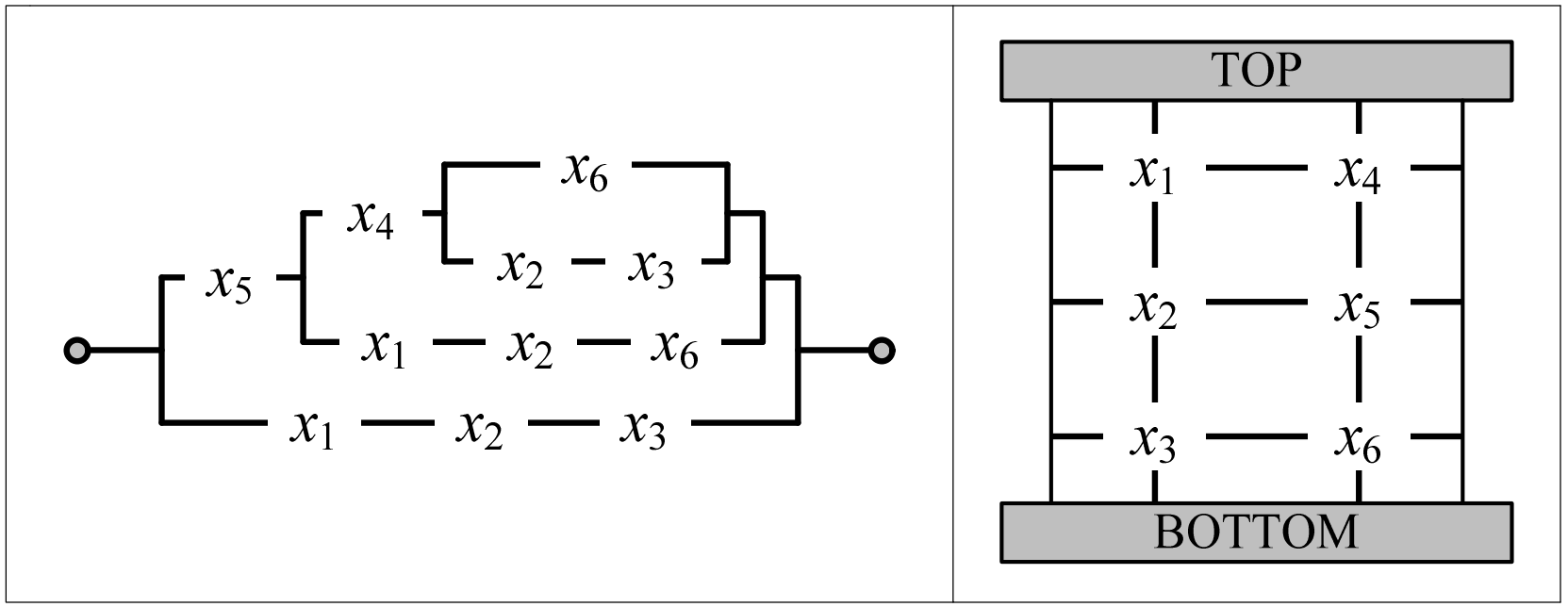
Parallel: $x_1 + x_2$



Series: $x_1 . x_2$



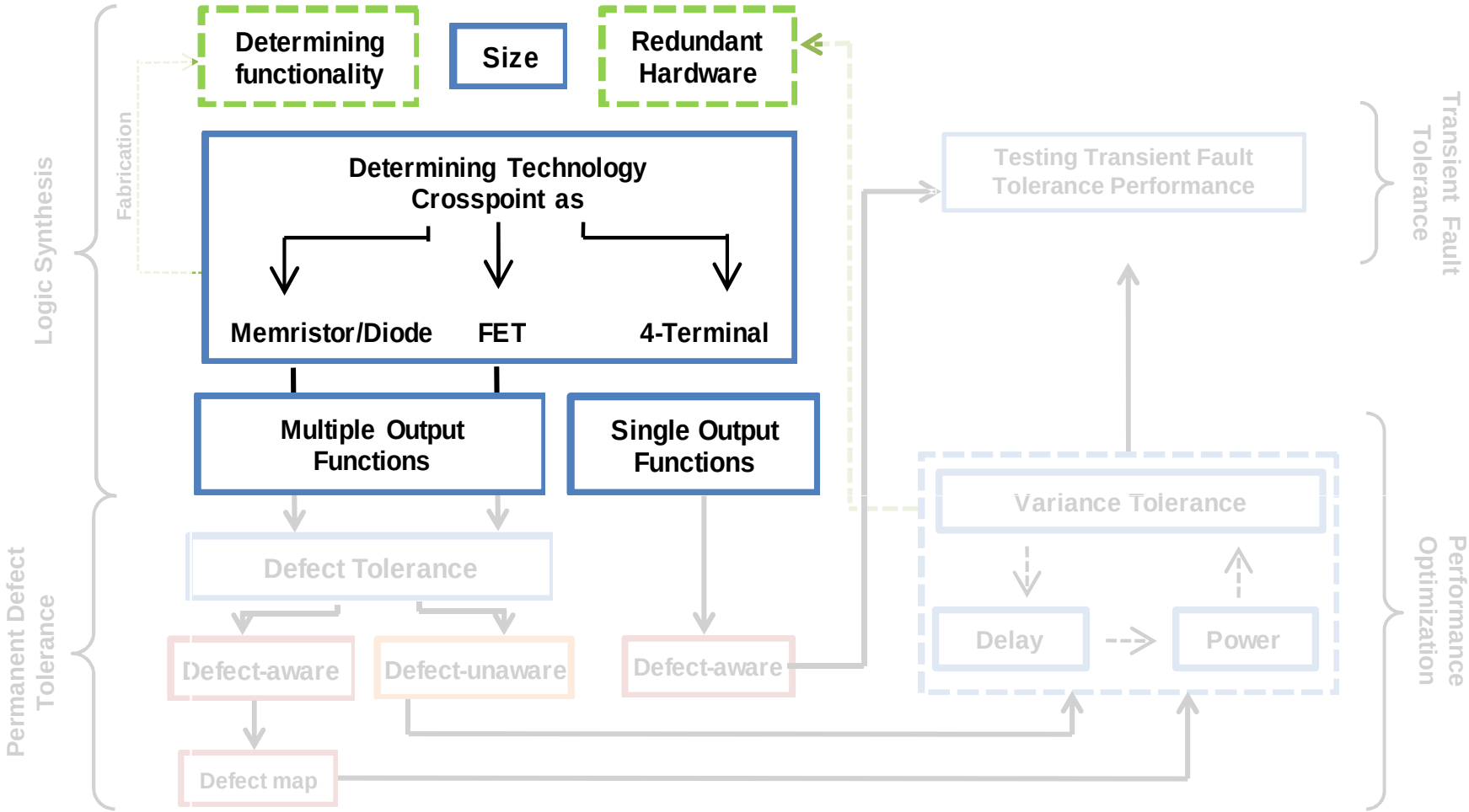
Two-terminal vs. Four-terminal



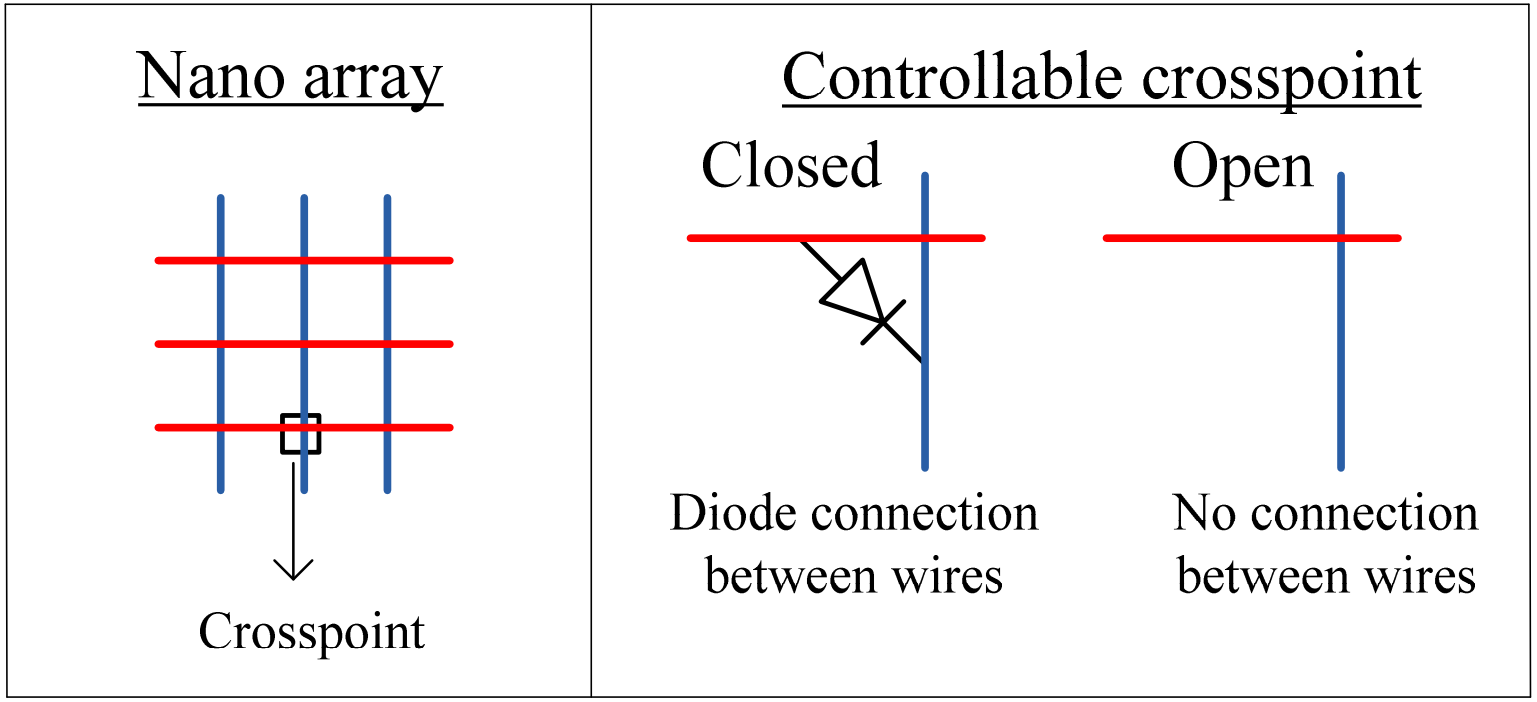
(a) (b)

What are the Boolean functions implemented in (a) ad (b)?

Logic Synthesis

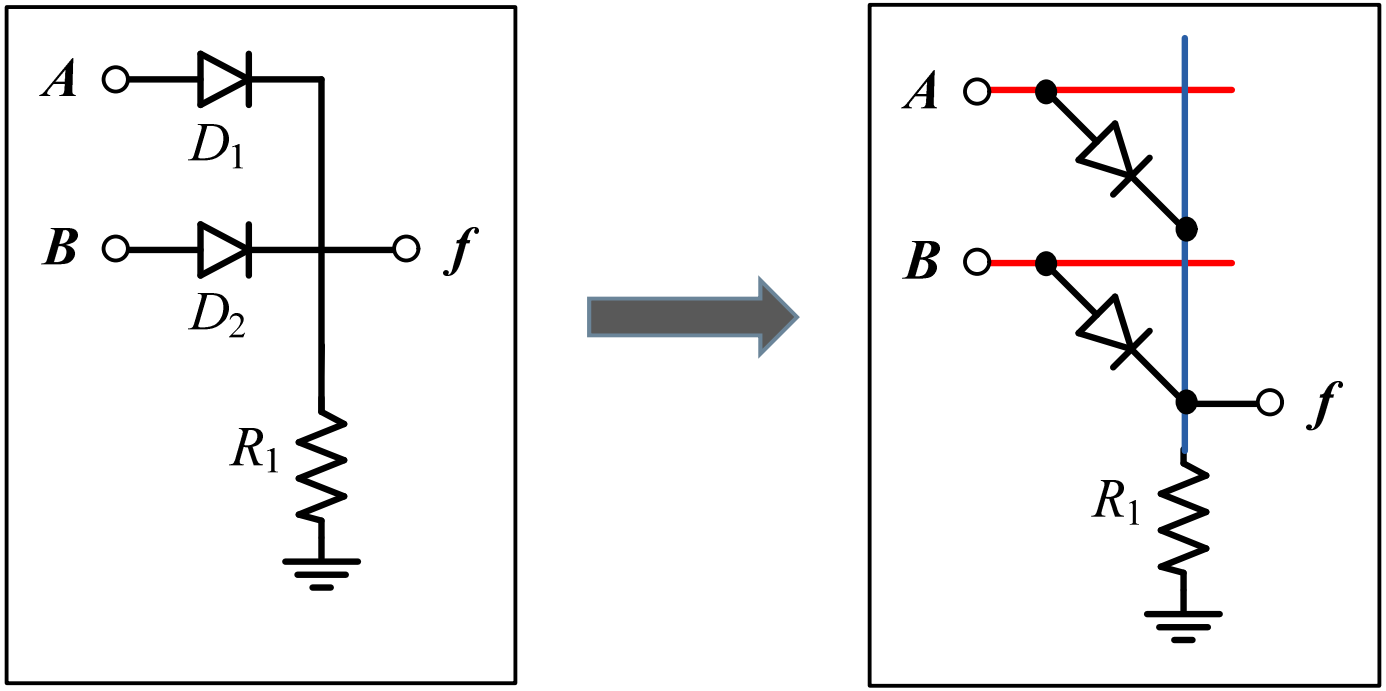


Diode/Memristor-based Model



Diode/Memristor-based Model

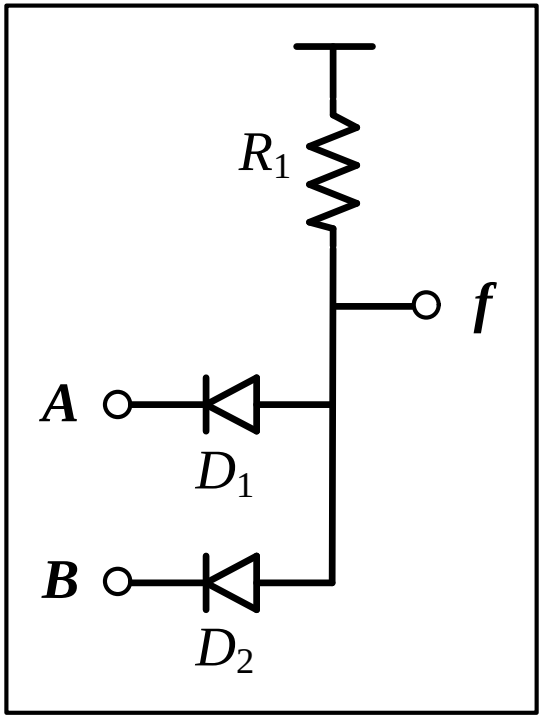
Example: Implement the Boolean function $f = A+B$ with **diode** based nanoarrays.



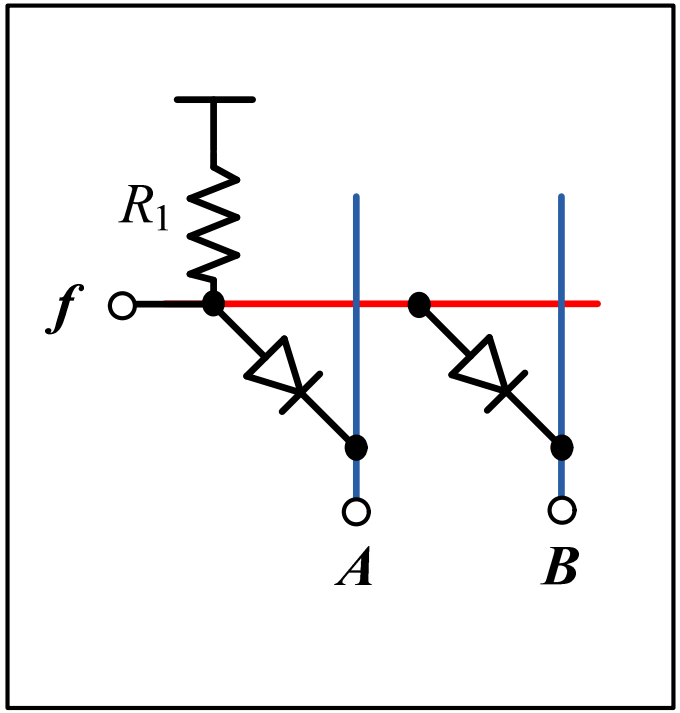
Diode-resistor logic

Diode/Memristor-based Model

Example: Implement the Boolean function $f = AB$ with **diode** based nanoarrays.

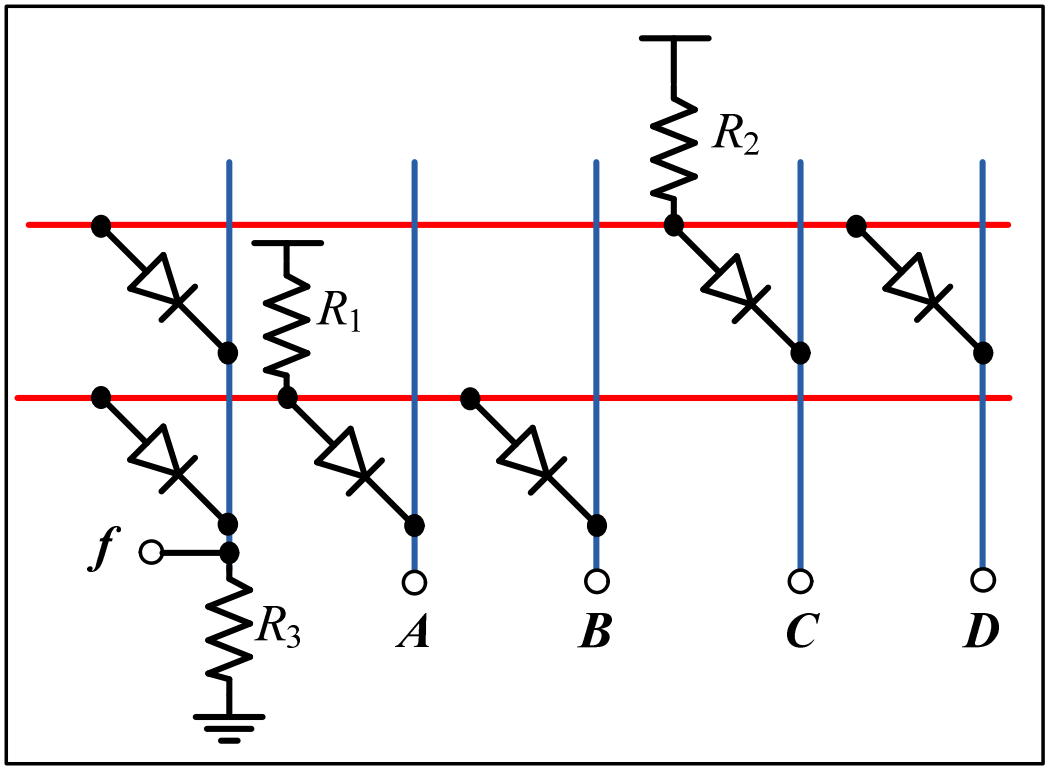


Diode-resistor logic

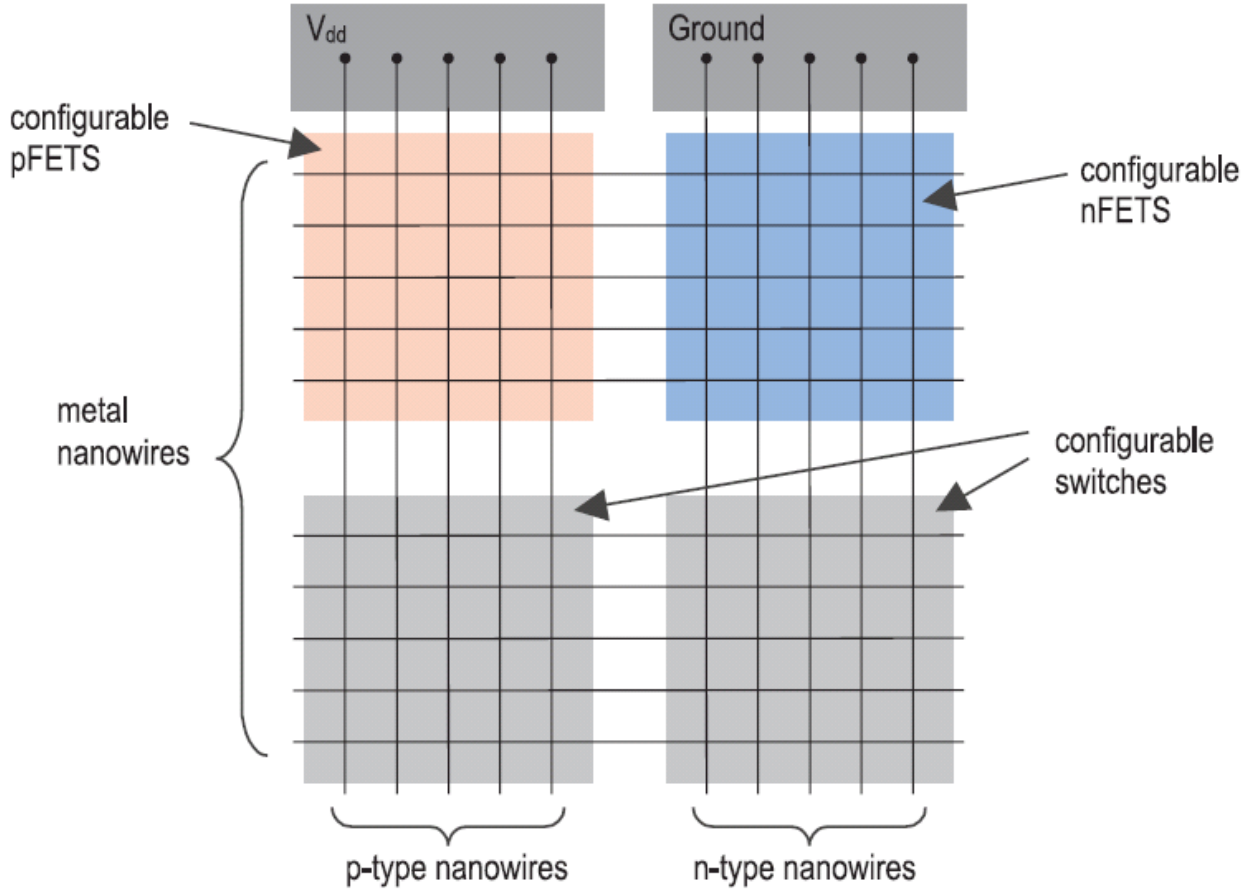


Diode/Memristor-based Model

Example: Implement the Boolean function $f = AB + CD$ with **diode** based nanoarrays.



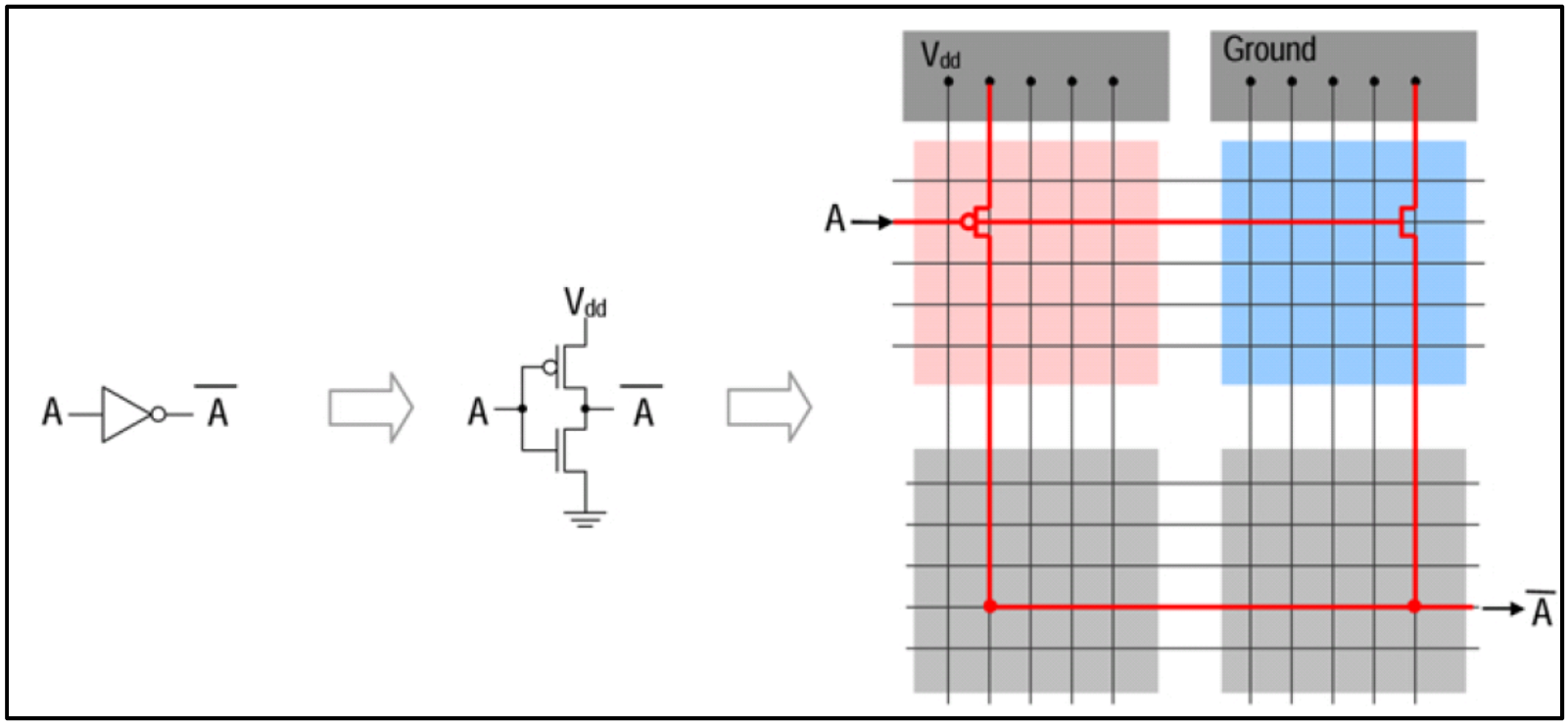
FET-based Model



From Snider, G., et al., (2004). CMOS-like logic in defective, nanoscale crossbars. *Nanotechnology*.

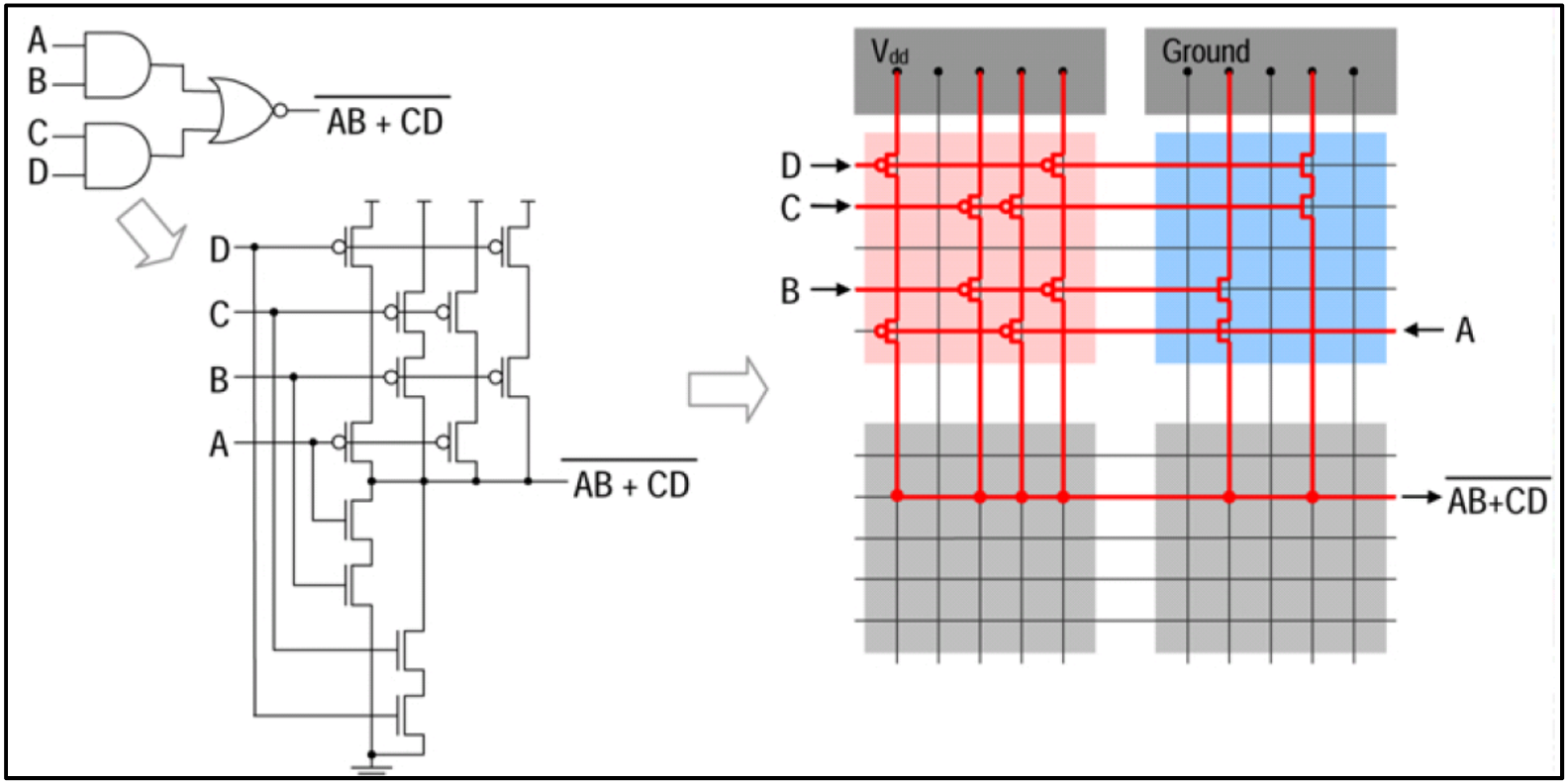
FET-based Model

Example: Implement the Boolean function $f = A'$ with **FET** based nanoarrays using **CMOS**-like logic.

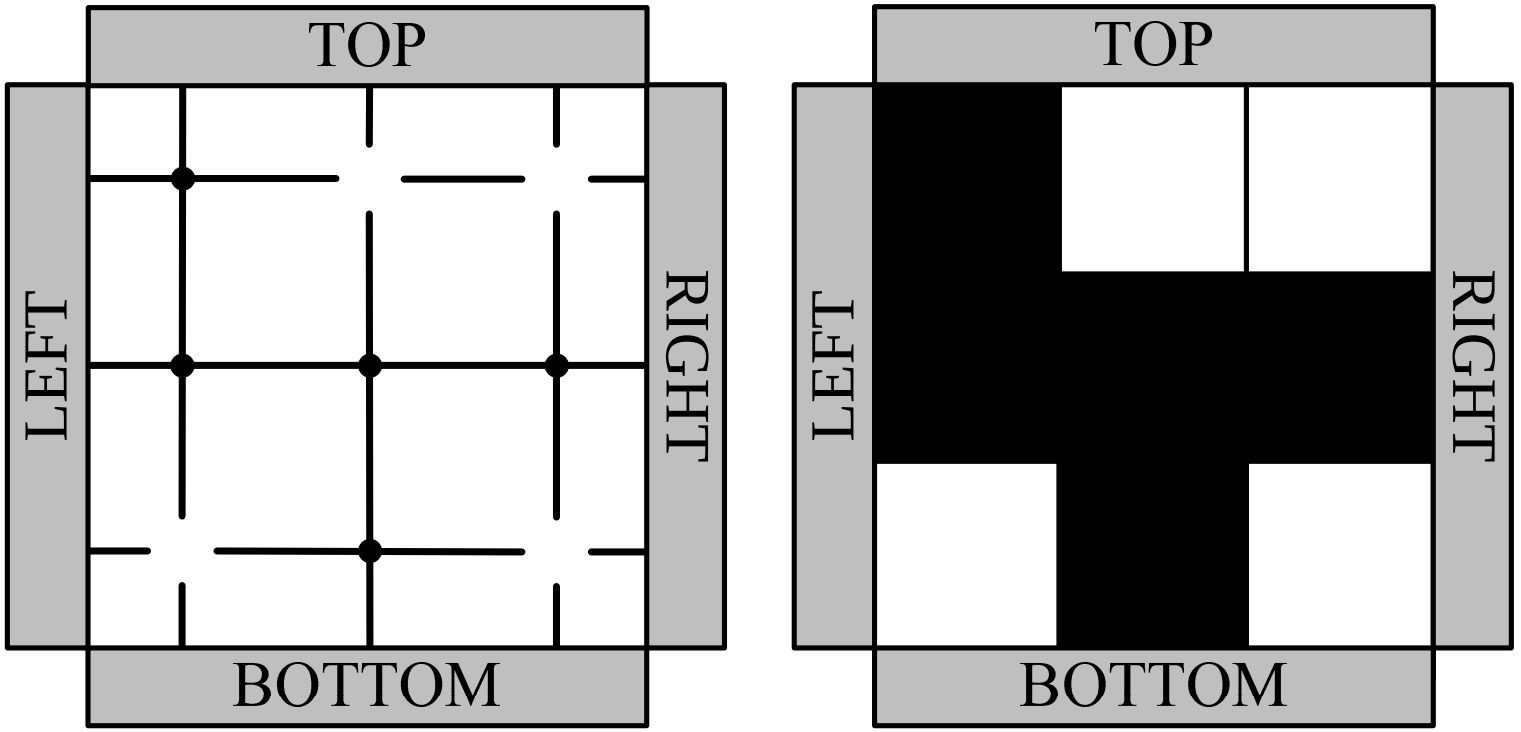


FET-based Model

Example: Implement the Boolean function $f = (AB + CD)'$ with **FET** based nanoarrays using **CMOS**-like logic.



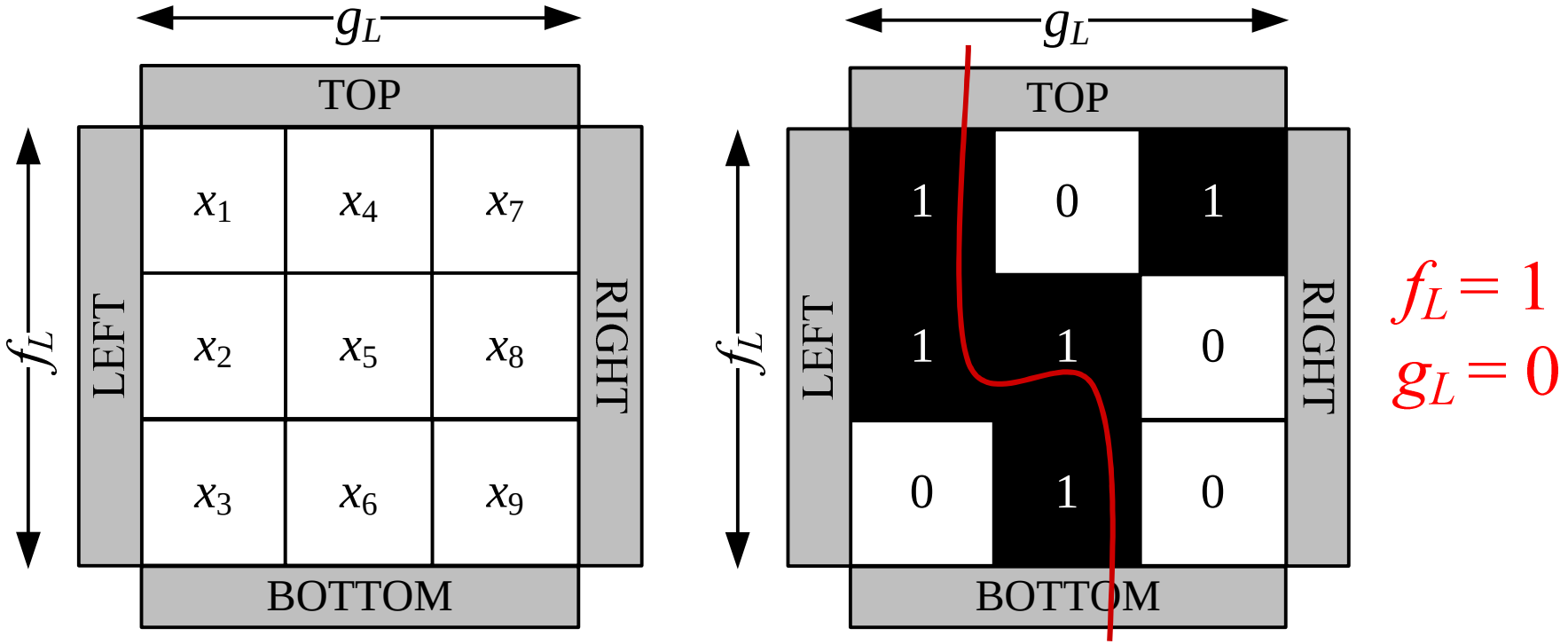
Four-terminal Switch-based Model



3 × 3 2D switching network and its lattice form

Four-terminal Switch-based Model

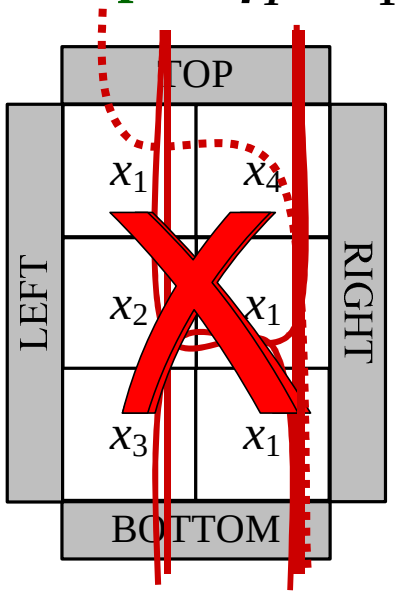
- Switches are controlled by Boolean literals.
- f_L evaluates to 1 iff there exists a top-to-bottom path.
- g_L evaluates to 1 iff there exists a left-to-right path.

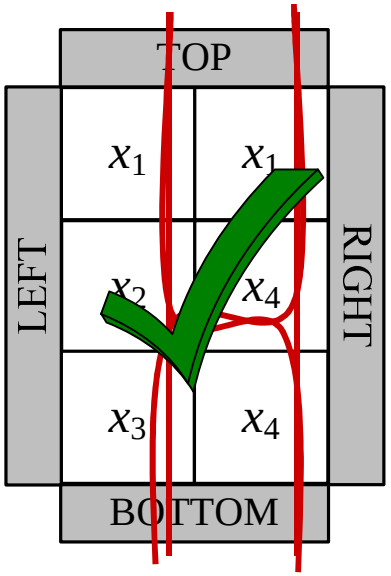


Logic Synthesis Problem

How can we implement a given target Boolean function f_T with a lattice of four-terminal switches?

Example: $f_T = x_1x_2x_3+x_1x_4$





$f_{L1} = x_1x_2x_3 + x_1x_4 + x_1x_2 + x_1x_2x_3x_4$

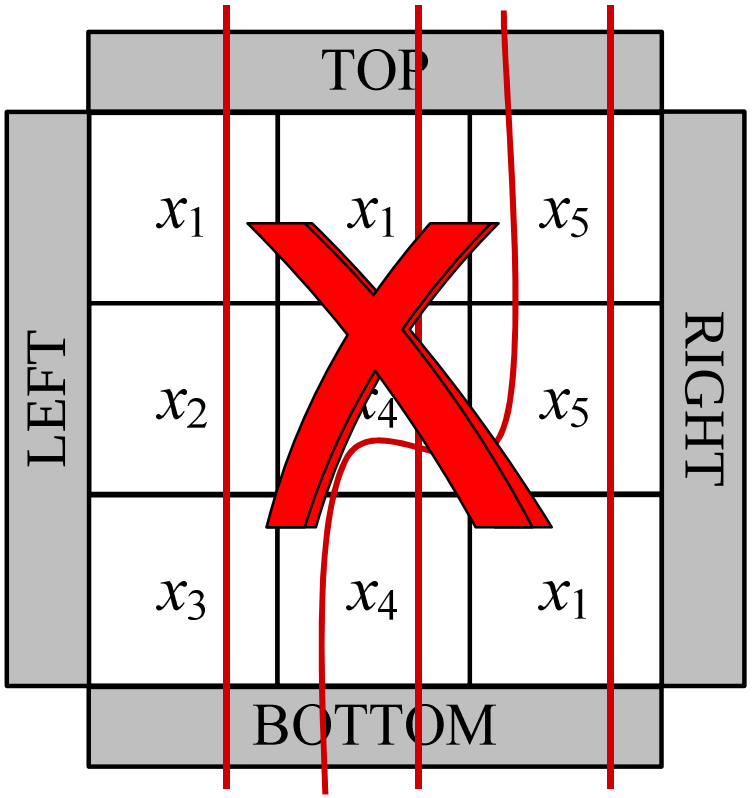
$f_{L1} = x_1x_2 + x_1x_4$

$f_{L2} = x_1x_2x_3 + x_1x_4 + x_1x_2x_4 + x_1x_2x_3x_4$

$f_{L2} = x_1x_2x_3 + x_1x_4$

Logic Synthesis Problem

Example: $f_T = x_1x_2x_3 + x_1x_4 + x_1x_5$



9 TOP-TO-BOTTOM PATHS!

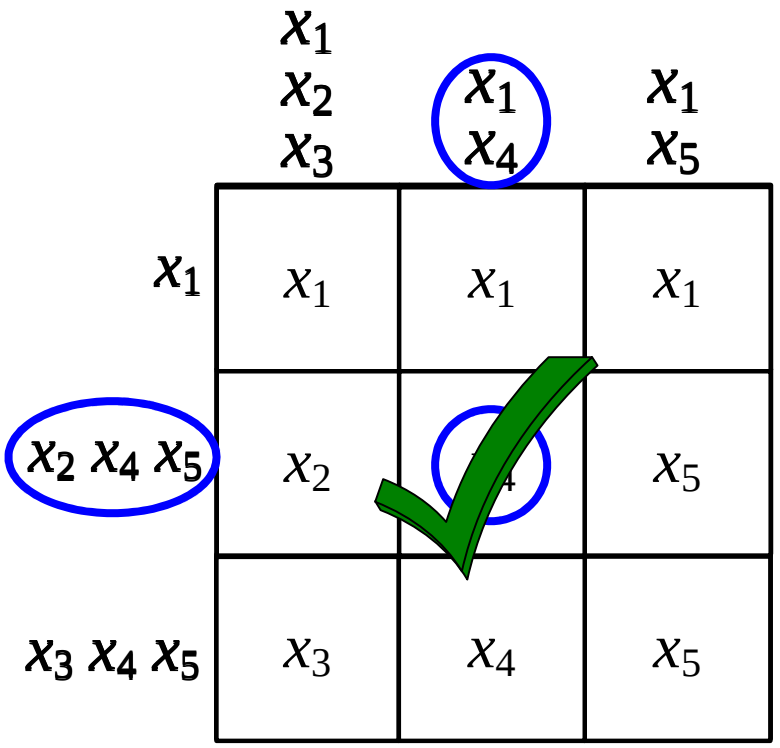
Synthesis Method

Example: $f_T = x_1x_2x_3+x_1x_4+x_1x_5$

- Start with f_T and its dual.
- Assign each product of f_T to a column.
- Assign each product of $f_T{}^D$ to a row.
- Compute an intersection set for each site.
- Arbitrarily select a literal from an intersection set and assign it to the corresponding site.

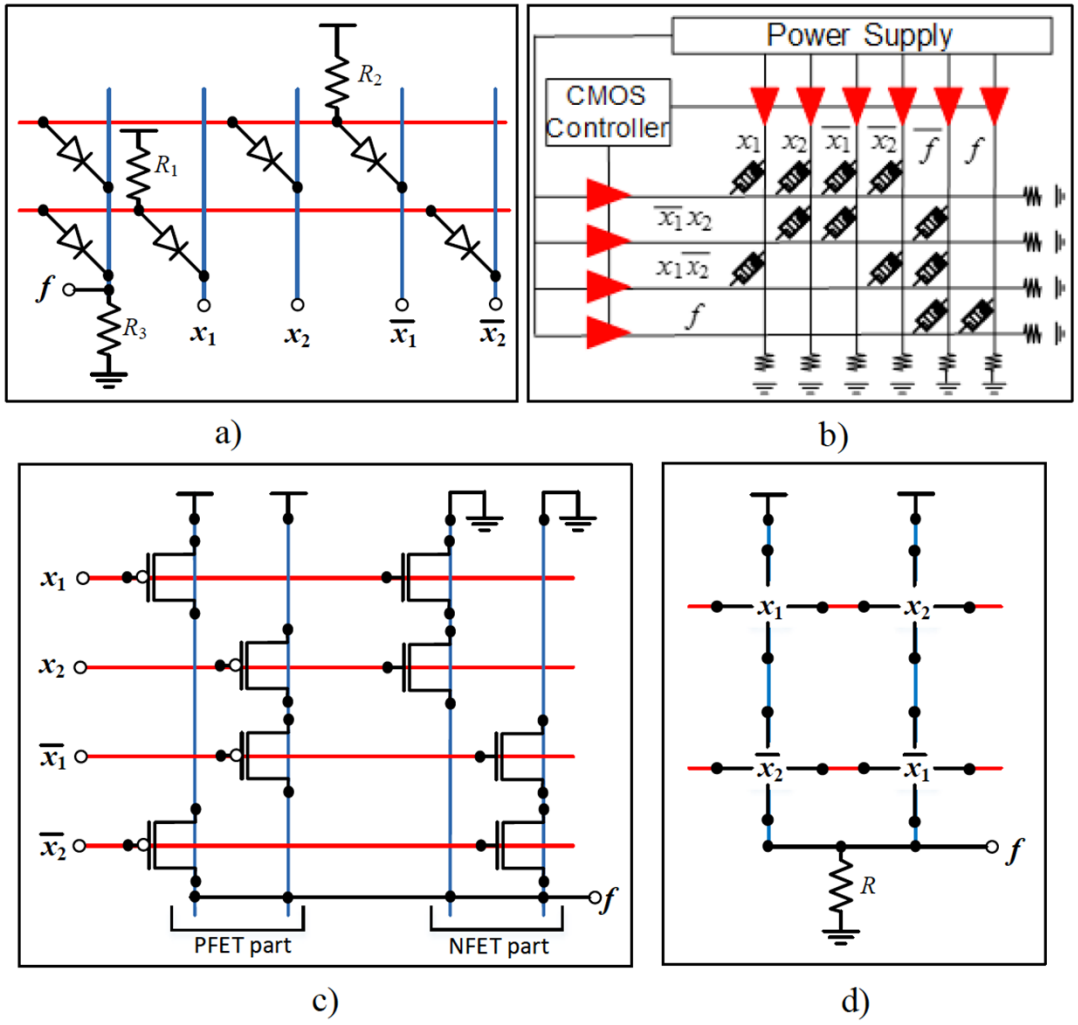
$f_T{}^D = (x_1+x_2+x_3)(x_1+x_4)(x_1+x_5)$

$f_T{}^D = x_1 + x_2x_4x_5 + x_3x_4x_5$



Experimental Results

Implementation of f_{XOR2} with different nanocrossbar types

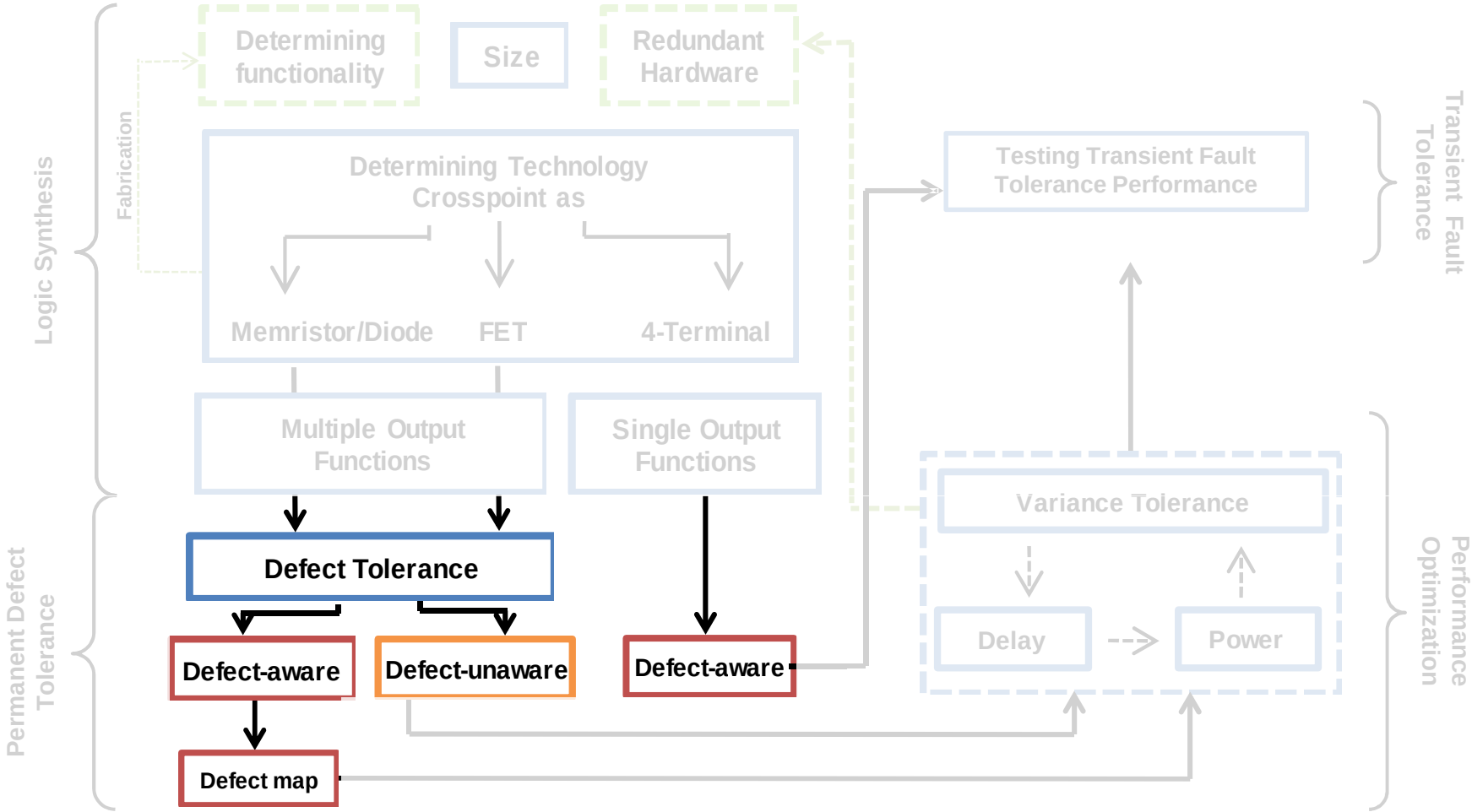


Experimental Results

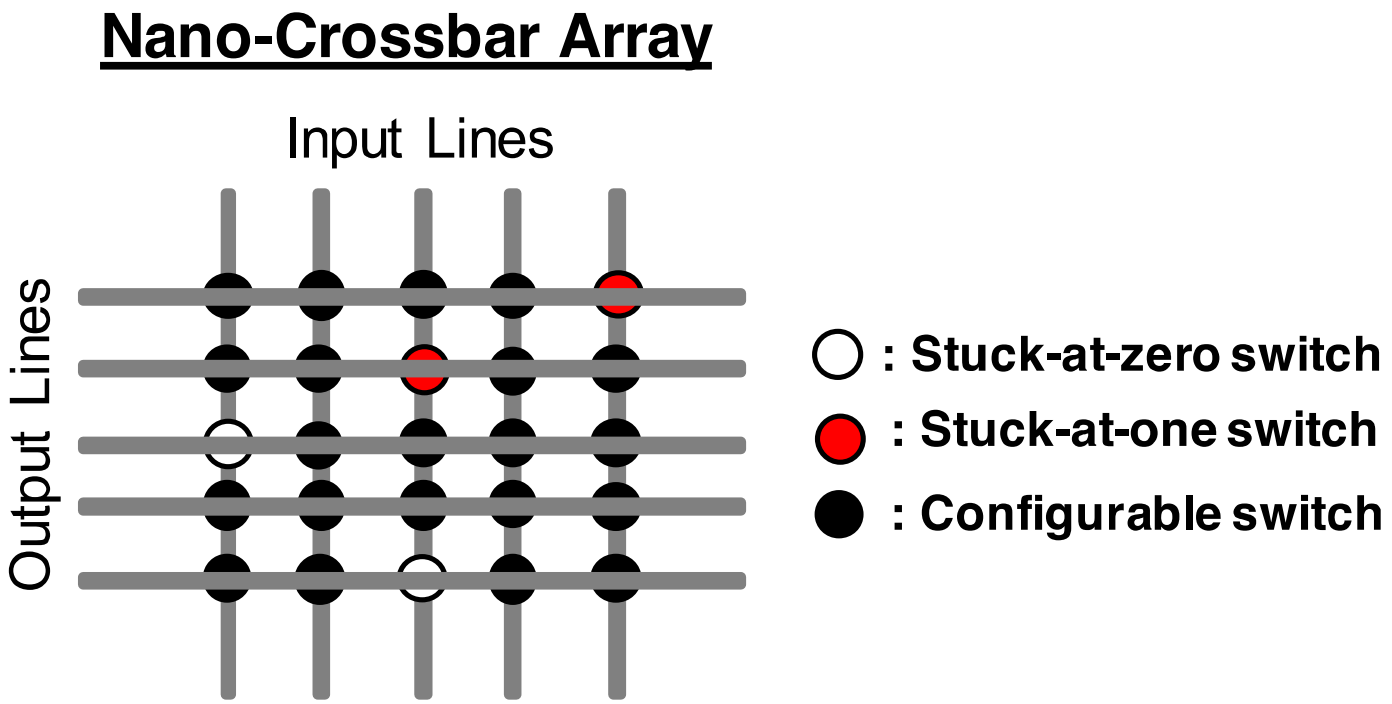
Type	Array Size Formulas
Diode	(number of products in f) x ("number of literals in f"+ 1)
FET-CMOS	(number of literals in f) x ("number of products in f" + "number of products in f^D")
Four-terminal	(number of products in f) x (number of products in f^D)

Benchmark	FET-CMOS	Diode	4-Terminal	Optimal 4-Terminal
Dc1 2	72	36	16	**12**
Dc1 5	35	15	12	**6**
Dc1 6	36	18	9	**6**
Ex5 31	156	104	32	**24**
Ex5 33	110	77	21	**21**
Ex5 46	81	54	18	**18**
Ex5 49	72	54	12	**12**
Ex5 50	81	63	14	**14**
Ex5 61	64	48	12	**12**
Ex5 62	49	35	10	**10**
Misex1 1	48	16	8	**8**
Misex1 2	132	55	35	**15**
Misex1 3	156	60	40	**24**
Misex1 4	121	44	28	**16**
Misex1 5	90	45	25	**15**
Misex1 6	143	66	42	**18**
Misex1 7	81	36	20	**15**
Mp2d 4	345	75	90	**24**
Newtag	108	72	32	**18**

Defect/Fault Tolerance



Defect/Fault Tolerance

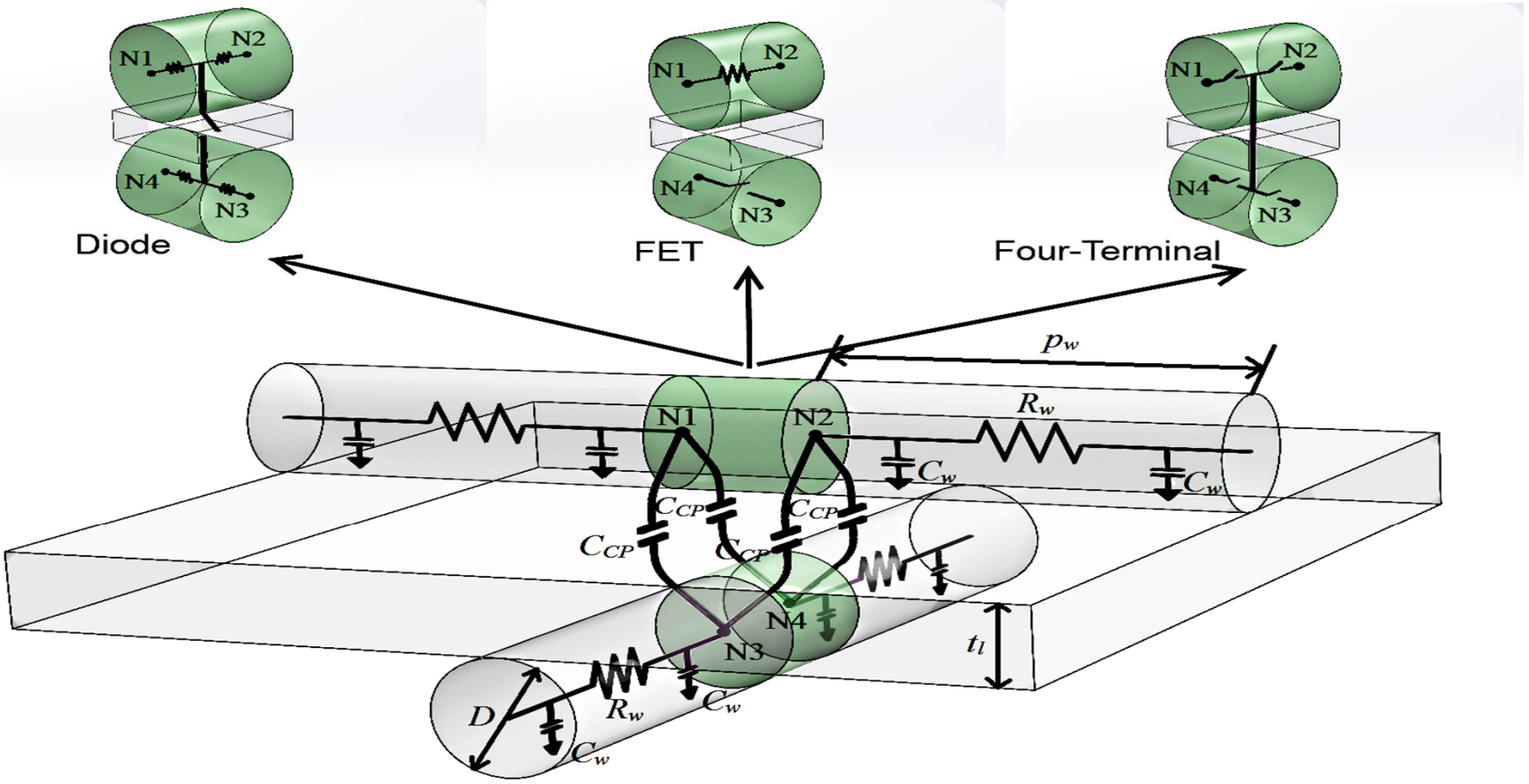


Permanent Faults occur mostly in fabrication and are tolerated in post-fabrication by redundancy and reconfigurability (mapping).
Transient Faults occur in field and are tolerated by redundancy

Defect/Fault Tolerance

- Defect tolerance is achieved by realizing a target logic function on a defective crossbar using row and column permutations
- For the worst-case, N!M! permutations are required to find a successful mapping for NXM crossbar.
  - **Defect-unaware** algorithms aim to find the largest possible kXk defect-free sub-crossbar from a defective NXN crossbar where $k \leq N$;
  - **Defect-aware** considers the defect characteristics (stuck-at-0 or stuck-at-1), then decide which switch to employ during the mapping.

Technology Development for FET/Diode/Memristor based Arrays



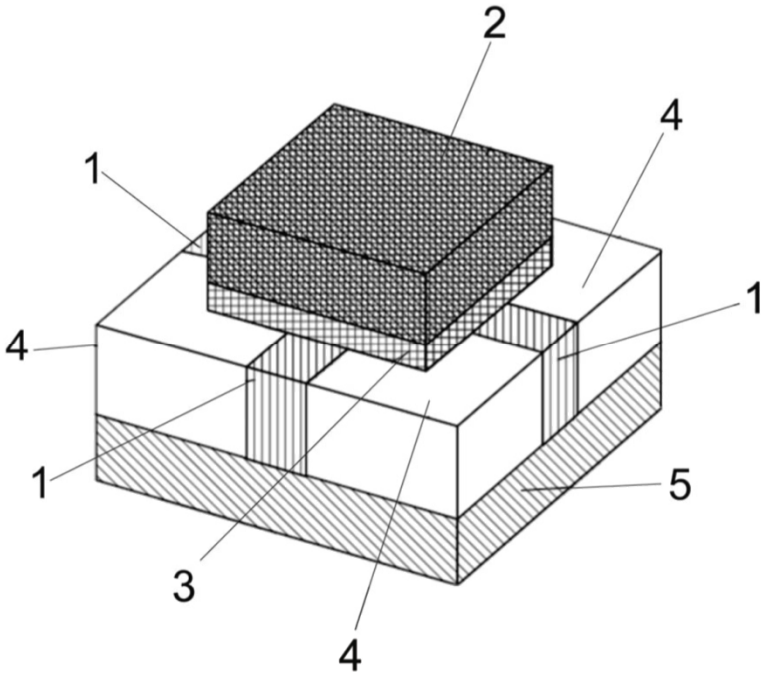
POST CMOS TECHNOLOGIES

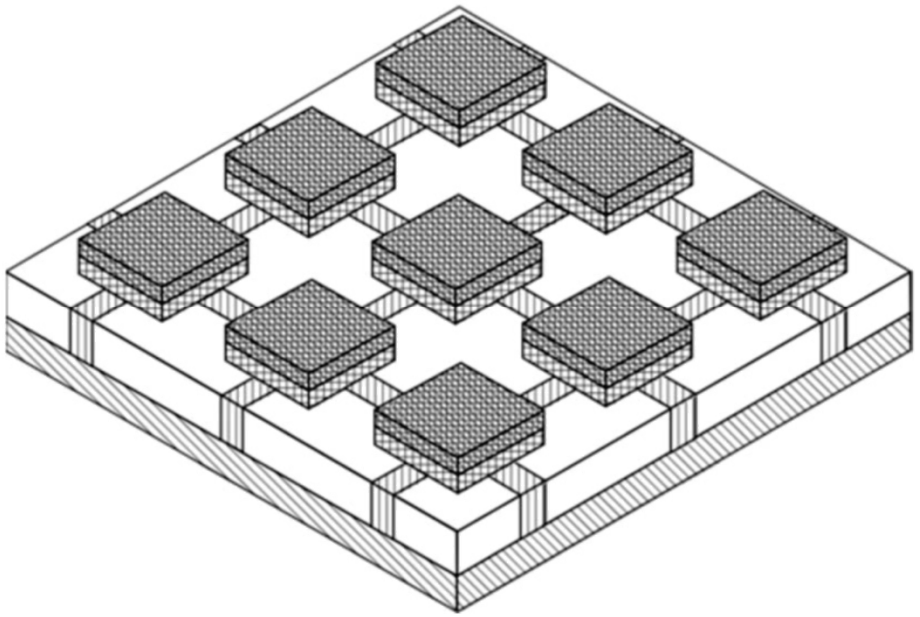
Technology Development for Four-Terminal Switch based Arrays

How about the technology?

- We propose CMOS-compatible technology with TCAD simulations
- By fitting the TCAD data to the standard CMOS current-voltage equations, we develop a Spice model of a four-terminal switch
- We are currently working toward the fabrication.

Device Structures



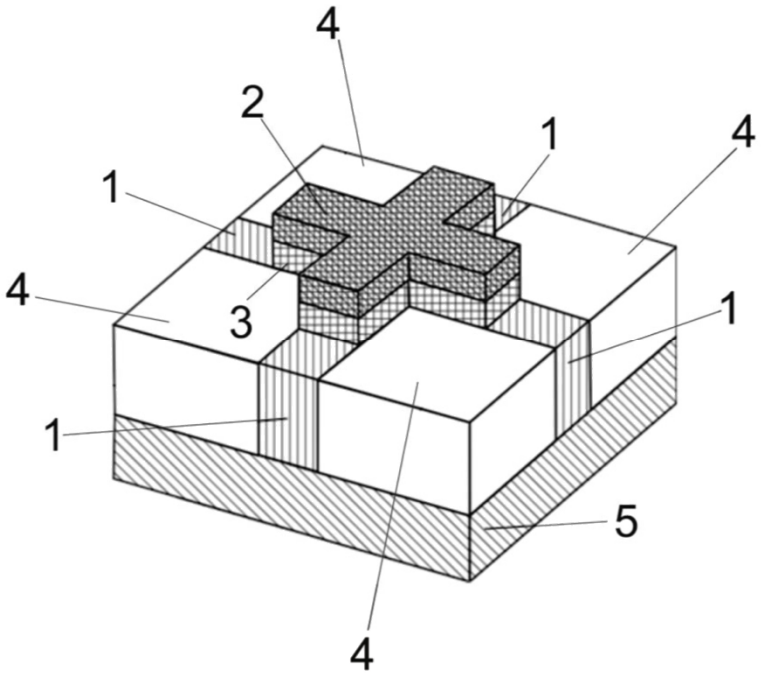


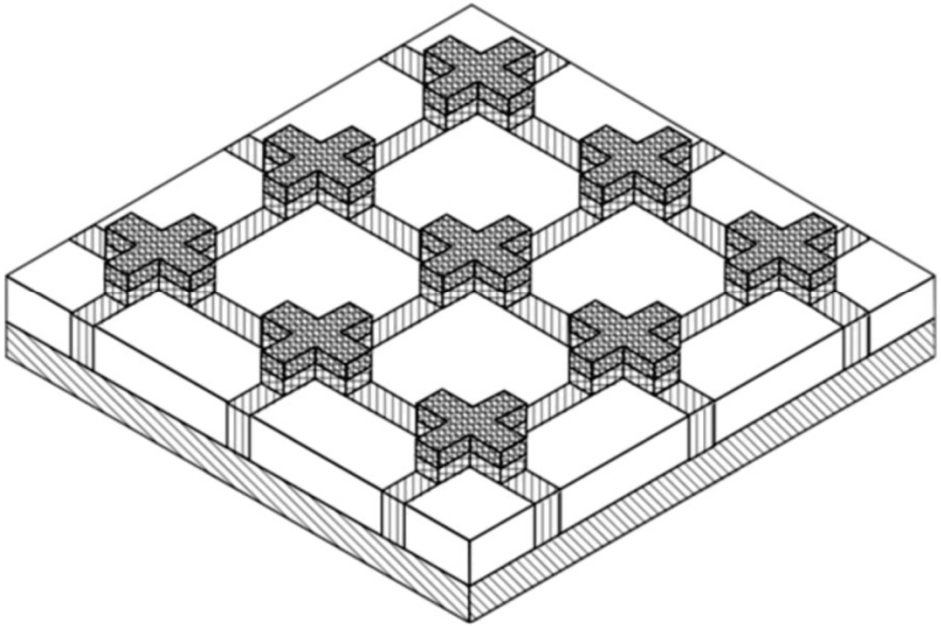
1: Diffusion region 2: Gate electrode 3. Gate insulator region

4: Local Oxidation of Silicon (LOCOS) or Shallow Trench Isolation (STI) layers

5: Bulk layer

Device Structures





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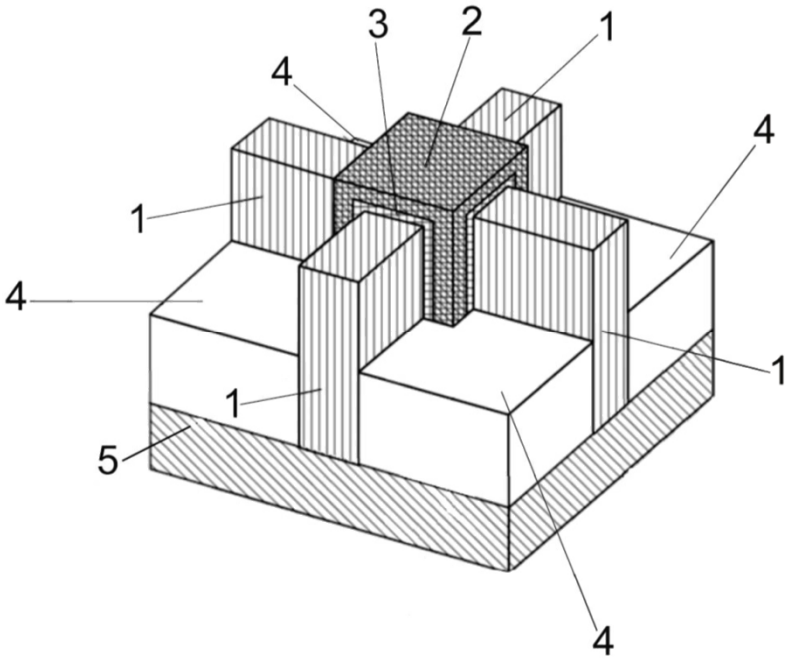

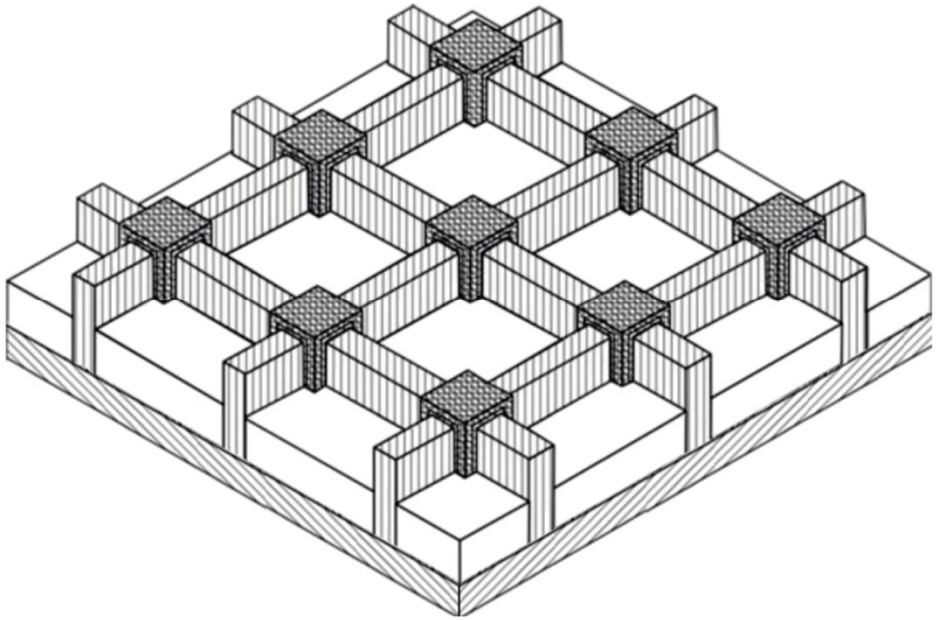

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THANK YOU!