

Challenges in Applying Nano/Micro Technologies to Sensor Devices

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Vladimir Laukhin, Institució Catalana de Recerca i Estudis Avançats, Spain

Henning Heuer, Fraunhofer Institut Zerstörungsfreie Prüfverfahren, Germany

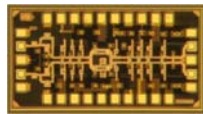
Salvatore Lombardo, CNR, Italy

Sergey Y. Yurish, IFSA, Spain

23 August 2011, SENSORDEVICES' 2011, Nice, France








Status and Challenges



- Technological limitation (below 100 nm, 28 nm ...)
- Analog and mixed circuits designs (ADC, OpAmp, etc.) becomes perceptibly more difficult
- Challenges are changes: from application driven to technologically driven
- Next step from MEMS sensors to NEMS sensors should be made

Electronics Development

Year				
1905	1947	1963	1974	2004
				
Vacuum Valve	Transistor	Operational amplifier	Analog-to-Digital Converter	Frequency-to-Digital Converter
Electronic Component				

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International Frequency Sensor Association • www.sensorsportal.com



Vision

- ✓ ● System design approach should be used (technological + structural algorithmic design approaches at the same time)
- ✓ ● New signal domain: frequency (period, time) instead of traditional analog or current
- ✓ ● New methods of measurements (MDC)
- ✓ ● New components (UFDC-1, USTI ICs)
- ✗ ● Trained engineering personnel

4

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Solutions: Technical & Others

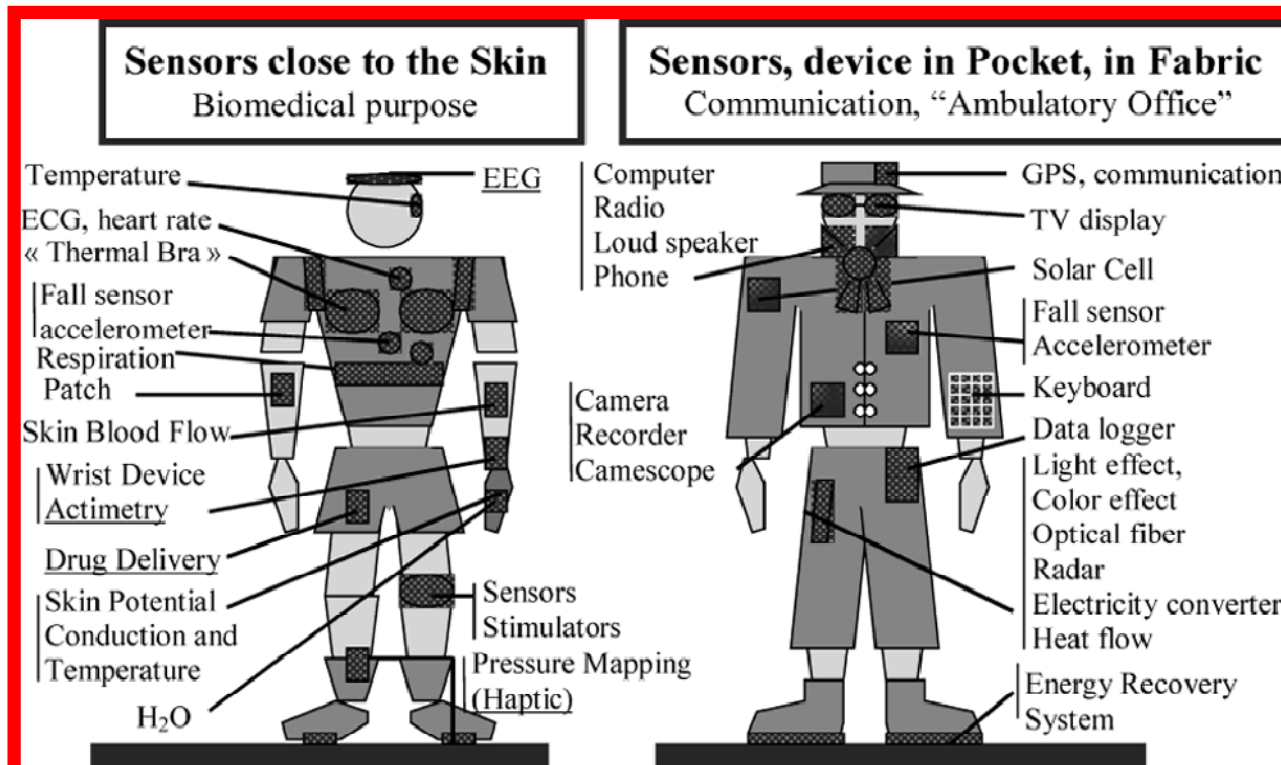


- Goodbye ADC, hello FDC !
- Frequency, duty-cycle or PWM sensors' outputs instead of traditional voltage or current outputs
- Road maps corrections: AMA Association for Sensor Technology, IEEE, EPoSS, etc.
- TEMPUS projects
- Advanced engineering training courses
- Other ?

Sensors for medical devices

"Citizen medicine" proposes to allow a patient to take care of his own healthcare at home or anywhere he goes.

Sensors and electronic circuits for biomedical and ambulatory office communications, which can be integrated in small catheters, in smart clothing, etc. are needed.

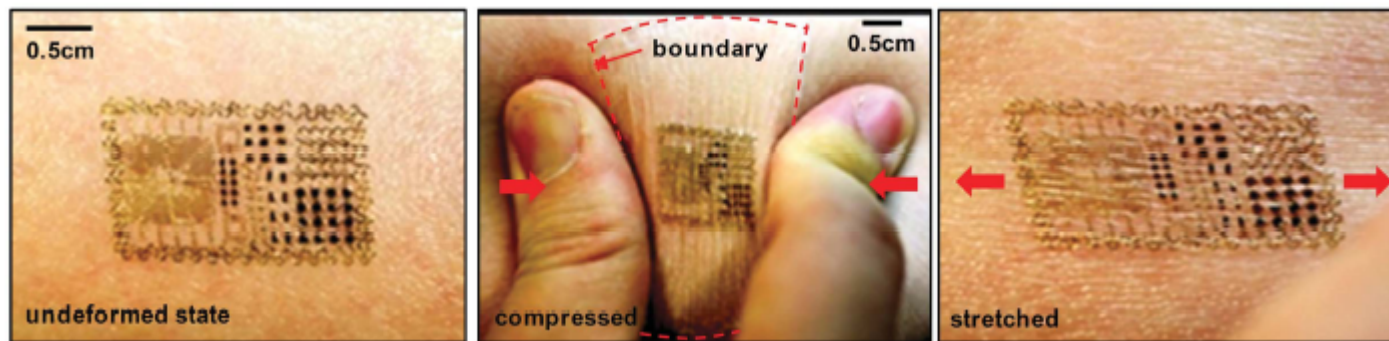


Sensors for medical devices

An electronic skin recently developed by **Kim *at al.*** and reported in the paper “**Epidermal Electronics**” [see [SCIENCE, V.333, P.838](#)] will help solve some problems for developing of monitoring devices.

One challenge for making these devices is to convert brittle semiconductors into more flexible form (e.g. silicon and germanium nanowires) placed on a supporting layer with appropriate properties.

The electronic skin must not be too thick, too rigid, too hard, or too heavy, but must have conformal contact, intimate integration, and adequate adhesion with the natural skin.



Multifunctional “epidermal electronic system” on skin: undeformed (left), compressed (middle), and stretched (right)

Sensors for medical devices

To achieve the goals of innovative biomedical monitoring technologies, sensors could be made of organic plastic conducting materials along with low cost processing steps

Our approach: Self-metallization of a flexible polycarbonate films with a highly strain resistive TTF-based organic metal, which could be considered as a perspective candidates for “Flexible Electronic Second Skin”...

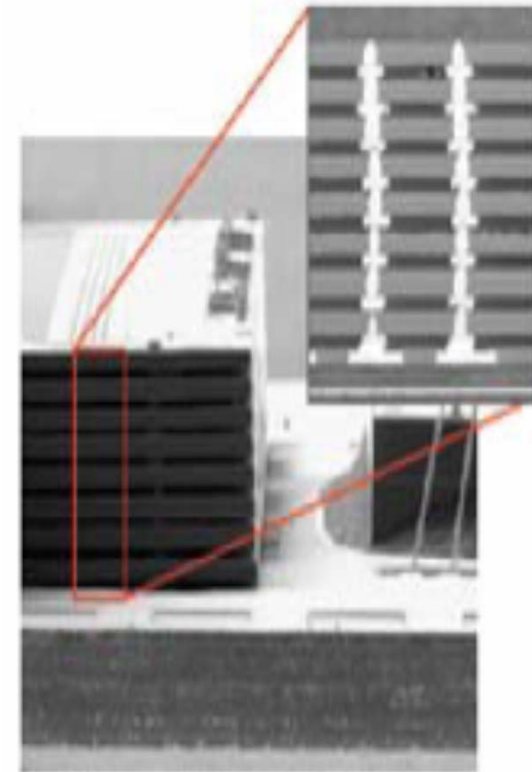
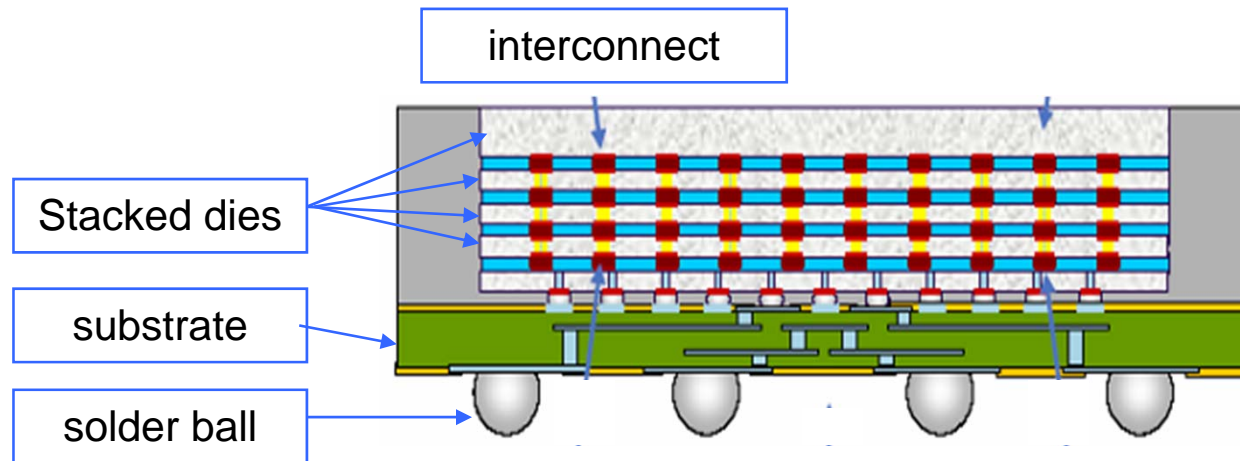
3D Integration by Through Silicon Via (TSV) Technology:

A revolution for designing matrix sensors?

henning.heuer@izfp-d.fraunhofer.de

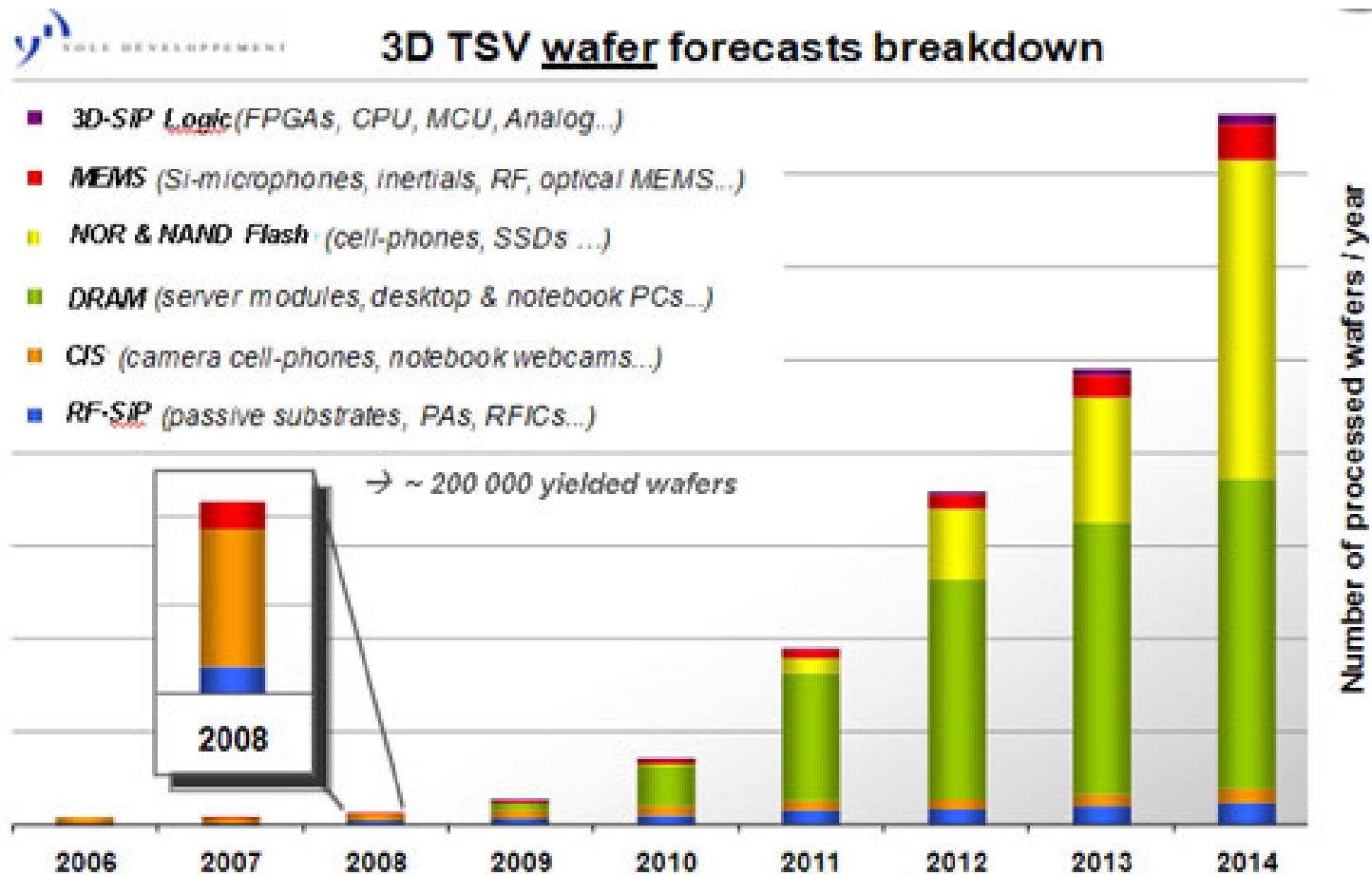
TSVs for 3d Integration in Microelectronics

Stacked Die:



Through Silicon Vias (TSVs)

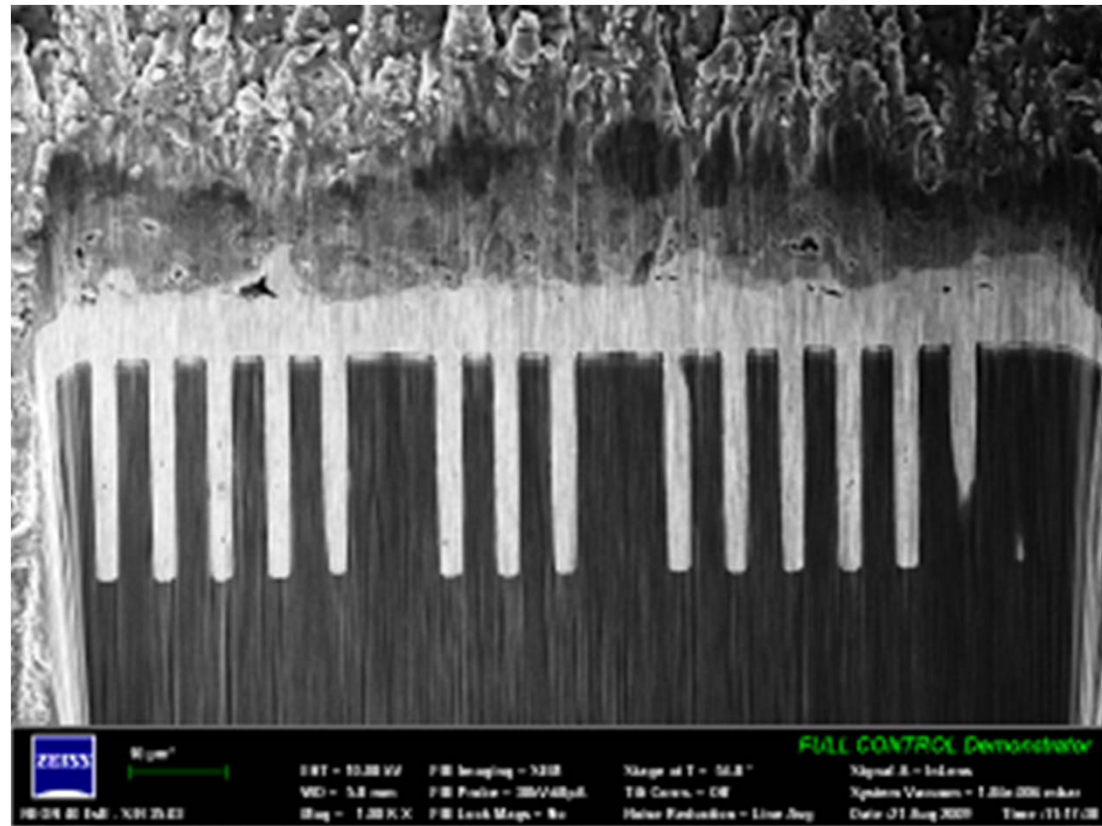
Trend



Source: YOLE, IMAPS 2008

TSV Analysis

Laserablation with subsequent FIB Milling

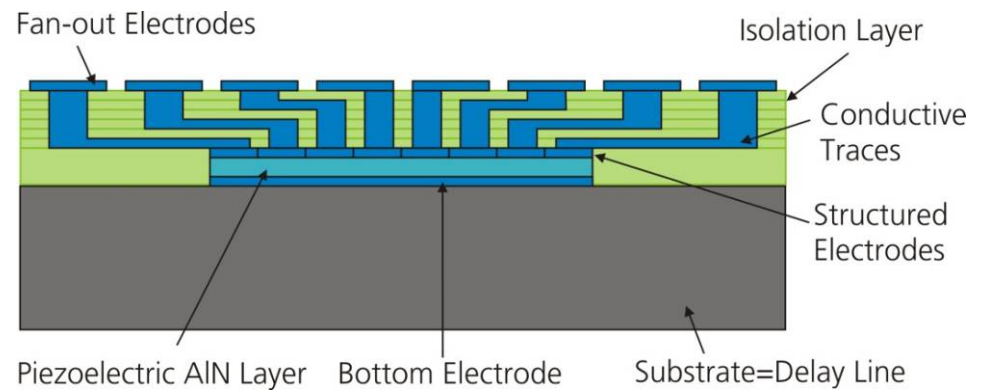
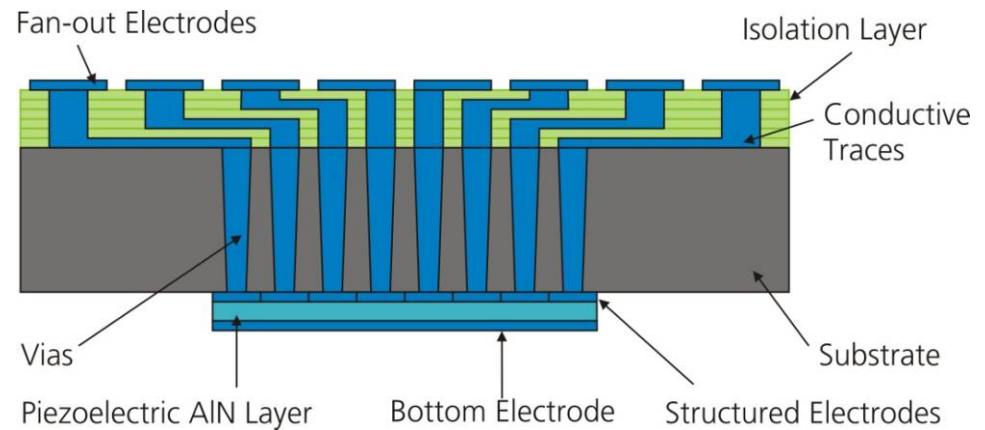


Matrix Transducer: Development of high resolving matrix sensors

Fan-out electrodes realized with multilayer thin film structure

Substrate could serve as delay line

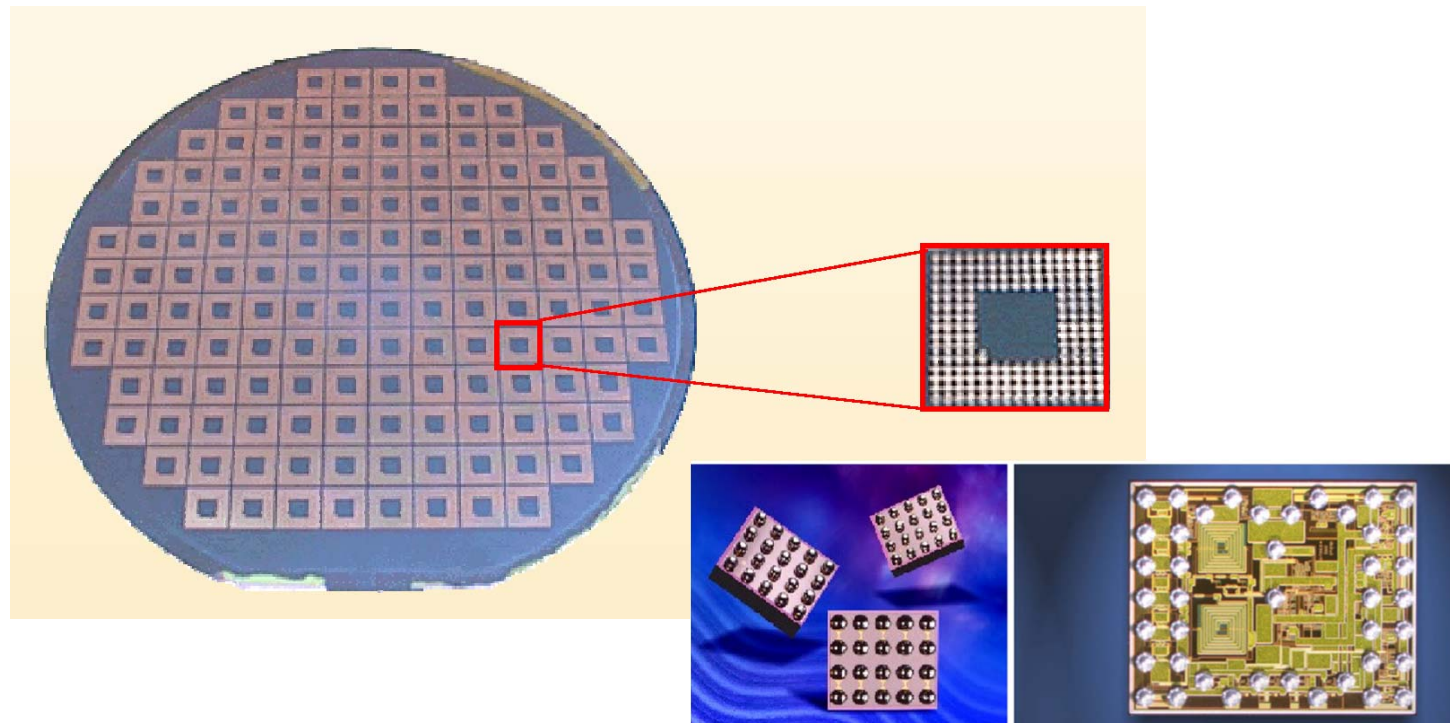
Wafer level packaging



Vision Transducer:

Development of a new high resolving matrix sensor system for the evaluation of micro-technical products

Transducer Chips with integrated preamplifier





Challenges in Applying Nano/Micro Technologies to Sensor Devices

Dr. Olivier Tesson



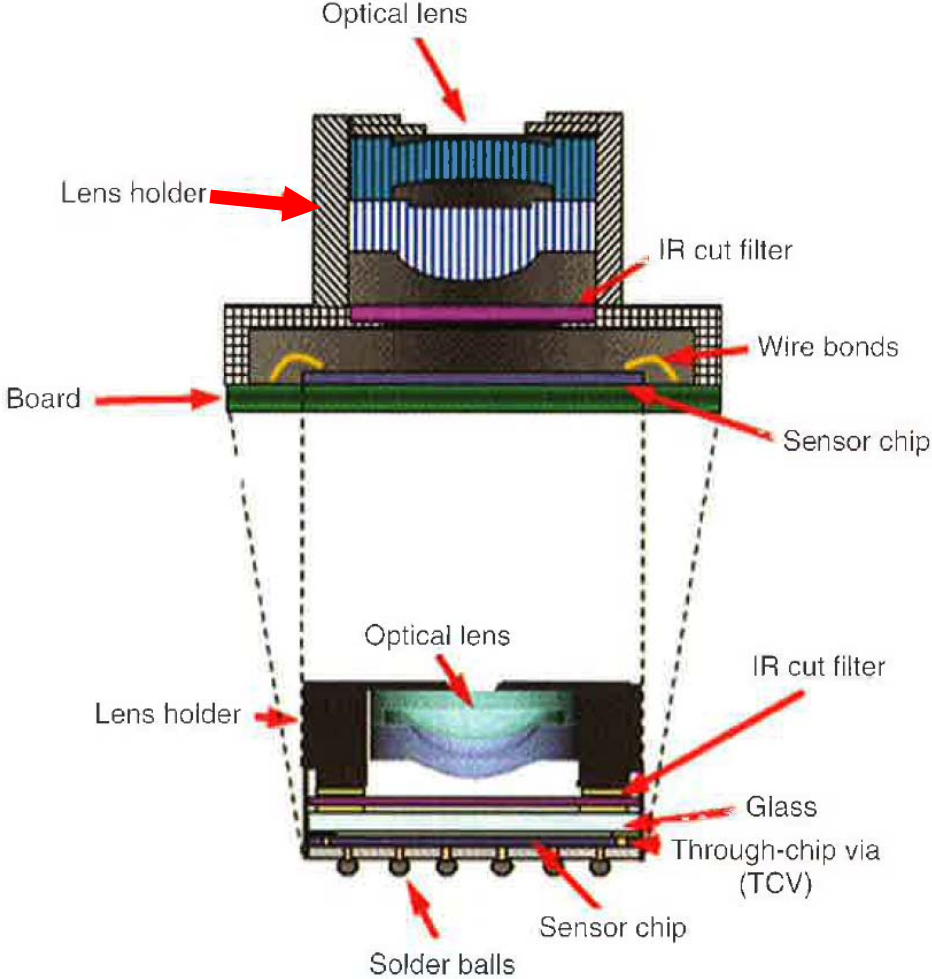
Caen, (France)

E-mail : olivier.tesson@nxp.com

4th International Conference on Advances in Circuits, Electronics and Micro-Electronics
(CENICS'2011)



Example 1- CMOS Image sensor (Toshiba)

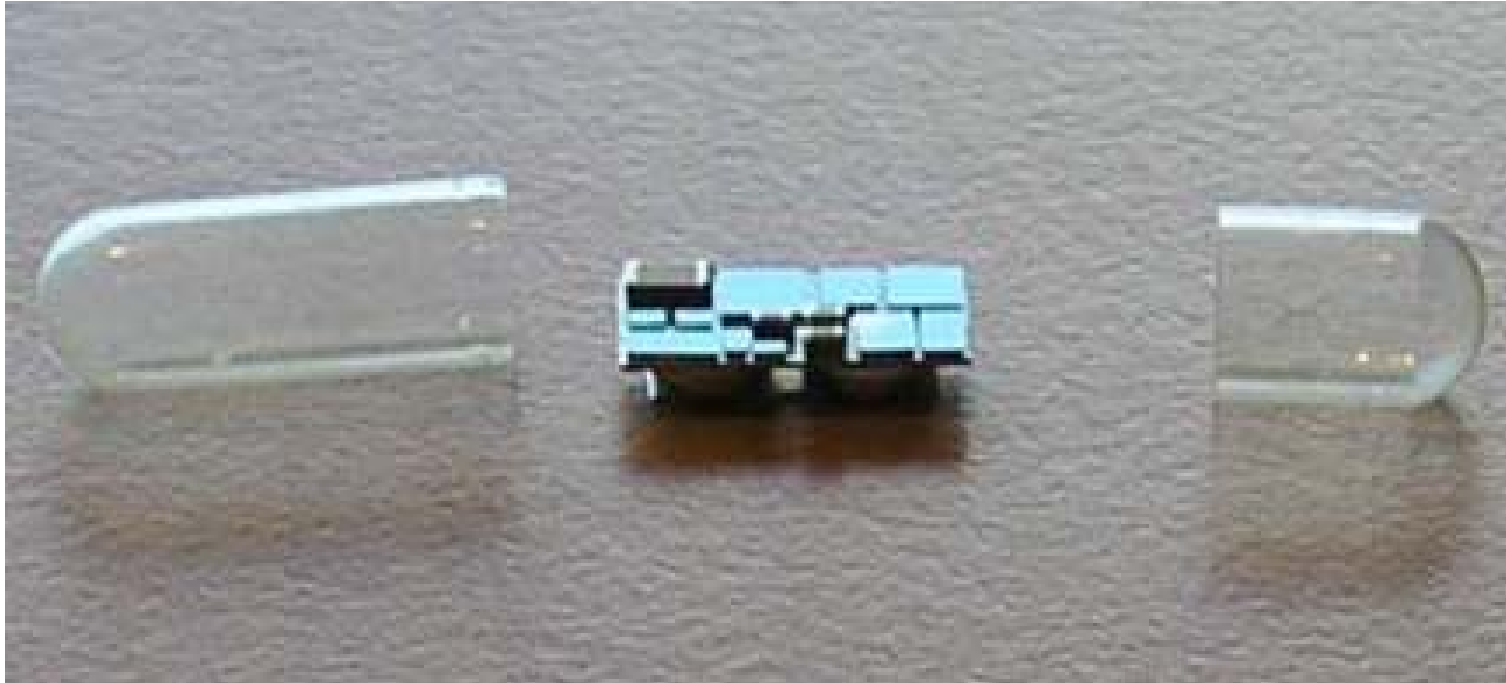


Moving from Wire bond solution to 3D IC integration

Source: John Lau



Example 2 – Temperature Sensor (*Ophthalmia*)



- *Temperature sensor + receiver + transmitter + batteries*
- *Medical system application*

Opportunities

- ▶ Small form factor:
 - Small system, reduced weight (PDA's, Mobile phones, MP3 player, Medical system)
 - Passive integration can be considered
- ▶ Improve performances:
 - Short interconnect → increase speed
- ▶ Cost!!:
 - Cheaper is better: system improvements does not require huge investments like for advanced CMOS technologies
- ▶ Reliability: very low ppm values already observed on an hybrid transceiver (*Murray, ESREF'07*)
- ▶ ...

Challenges

- ▶ Design guidelines still lacking for these systems
- ▶ Test methods and equipment are lacking
- ▶ (Thin) Wafer handling during processing
- ▶ These technology (3D-IC integration) is a challenge for materials science
 - Mechanical stress due to different material behaviour used in the stack
- ▶ Make the best use of 3D silicon processes and keep them simple
 - The sky is the limit to 3D integration and engineer imagination!
 - Develop the best suited assembly technology
- ▶ ...



Unconventional computing →

Chemical computing →

Computing with complicated/functional molecules →

Biomolecular computing →

Enzymatic computing ↔ Applications

Noise sources →

Noise reduction →

Gate design →

Network design ↔ Applications

Modeling enzyme-catalyzed biochemical reactions

Novel sensor design



*Various paradigms for scalable, supposedly
“fault-tolerant” information processing:*

- digital electronic circuitry
- living things
- quantum parallelism
- “ensemble” parallelism

Examples:

laptop

rabbit

(?)

(?)

Biochemical computing:

information processing paradigm – *analog (?) / digital (?) circuitry (?)*;

tools – including the use of *biomolecules* (such as enzymes),
which offer the advantage of *specificity*

Possible applications of biochemical information processing:

- The aim is not to replace the electronic computers, but rather to offer multi-step *information processing without wires and batteries*
- ***Multiple-input sensing*** resulting in response/actuation of the “digital” (threshold) nature
- ***Compound “test strips”***
- ***“Decision-making” implantable biomedical devices***
- Coupling to *responsive / “smart”* materials or electrodes

Towards Biosensing Strategies Based on Biochemical Logic Systems,
E. Katz, V. Privman and **J. Wang**, in: Proc. Conf. ICQNM 2010, edited by
V. Ovchinnikov and V. Privman (IEEE Comp. Soc. Conf. Publ. Serv., Los
Alamitos, California, 2010), pages 1-9,
<http://dx.doi.org/10.1109/ICQNM.2010.8>

*Enzyme-Based Logic Systems for Information
Processing*, **E. Katz** and V. Privman, Chem. Soc.
Rev. 39, 1835-1857 (2010),
<http://dx.doi.org/10.1039/B806038J>

*Control of Noise in Chemical and Biochemical
Information Processing*, V. Privman, Israel J.
Chem. 51, 118-131 (2011),
<http://dx.doi.org/10.1002/ijch.201000066>

All the listed
and several
other articles
are available at
the web site.

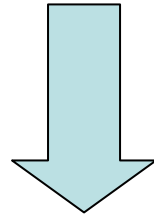
Silicon Nanostructures for Advanced Devices

Salvatore Lombardo

Consiglio Nazionale delle Ricerche (CNR)

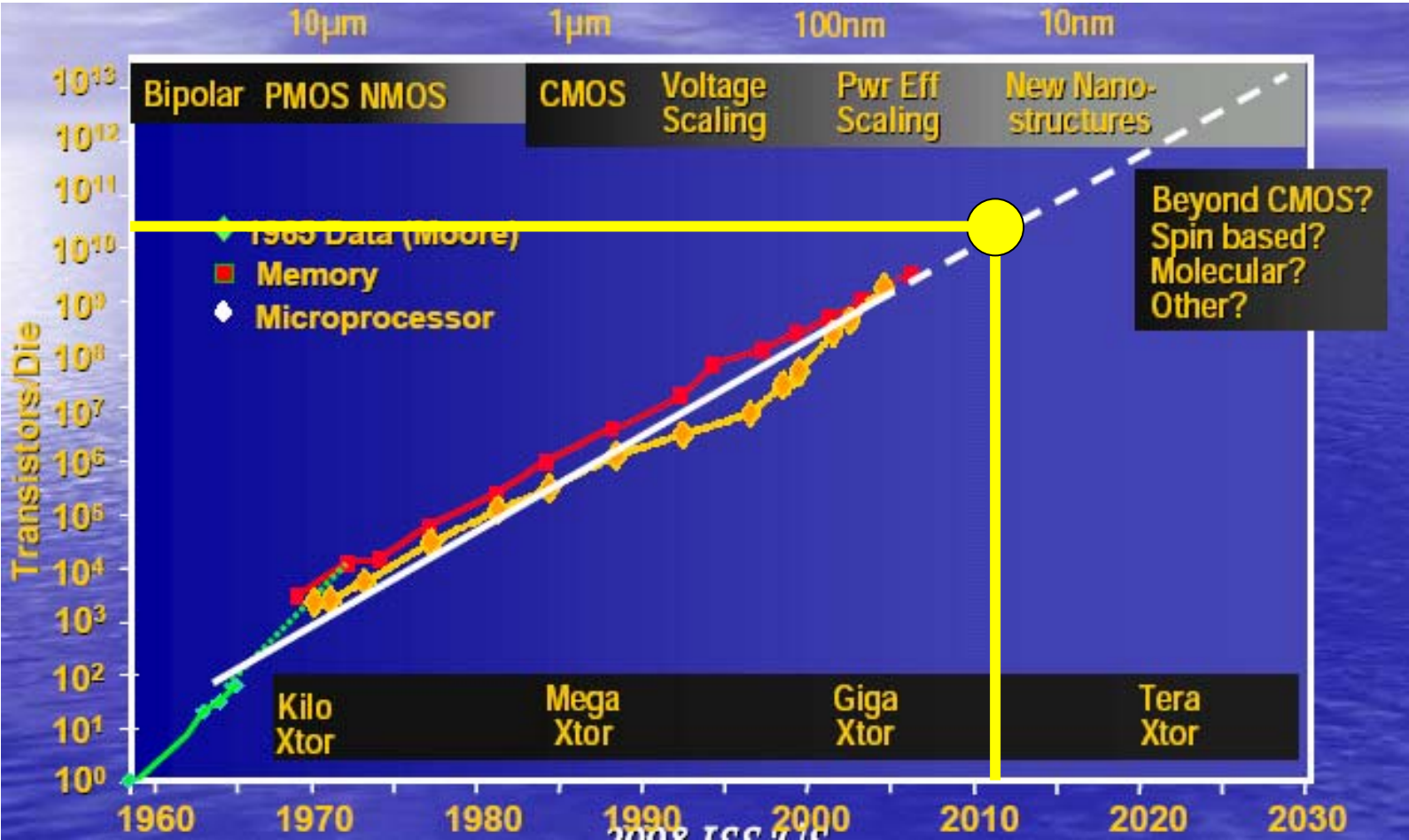
Istituto per la Microelettronica e Microsistemi (IMM), Catania, ITALY

Silicon for Microelectronics



Nanostructures (up to \approx 5 nm)

Moore's Law



from: "Overcoming the Red Brick Walls", Paolo Gargini, 2008 ISS US

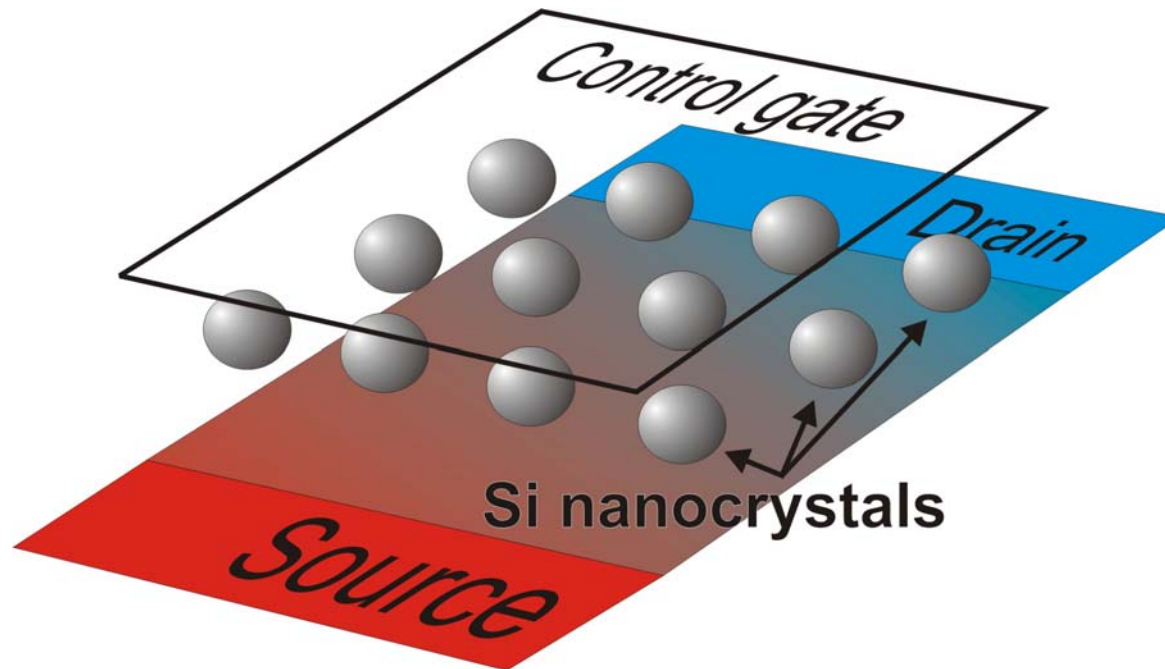


FLASH, DRAM, & MPU 1/2 Pitch

<i>Table ORTC-1 ITRS Technology Trend Targets</i>		[including PIDS 2011 Roadmap Flash and DRAM Trend Driver Proposals]							
<i>Year of Production</i>		2009	2010	2011	2012	2013	2014	2015	2016
<u>2010 PIDS Projection based on survey data</u>	<u>Flash 1/2 Pitch (nm) (un-contacted Poly)(f) [B]</u>	N/A	<u>26</u>	<u>24</u>	<u>22</u>	<u>20</u>	<u>19</u>	<u>18</u>	<u>16</u>
<u>2010 PIDS Projection based on survey data</u>	<u>DRAM 1/2 Pitch (nm) (contacted) [D]</u>	N/A	<u>42</u>	<u>36</u>	<u>31</u>	<u>28</u>	<u>25</u>	<u>24.0</u>	<u>21.0</u>
	<i>MPU/ASIC Metal 1 (M1) 1/2 Pitch (nm)[1,2]</i>	54	45	38	32	27	24	21	18.9
	<i>MPU Printed Gate Length (GLpr) (nm) ††[1]</i>	47	41	35	31	28	25	22	19.8
	<i>MPU Physical Gate Length (GLph) (nm)[1]</i>	29	27	24	22	20	18	17	15.3
	<i>ASIC/Low Operating Power Printed Gate Length (nm) ††[1]</i>	54	47	41	35	31	25	22	19.8
	<i>ASIC/Low Operating Power Physical Gate Length (nm)[1]</i>	32	29	27	24	22	18	17	15.3

Source: THE INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: 2010 UPDATE

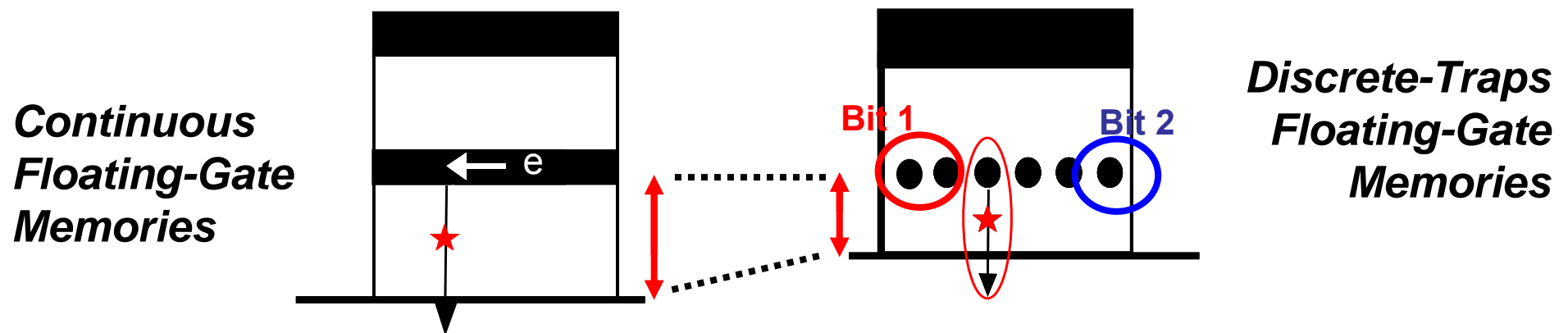
Use of Si dots for charge storage in FLASH



Use of Si dots for charge storage in FLASH

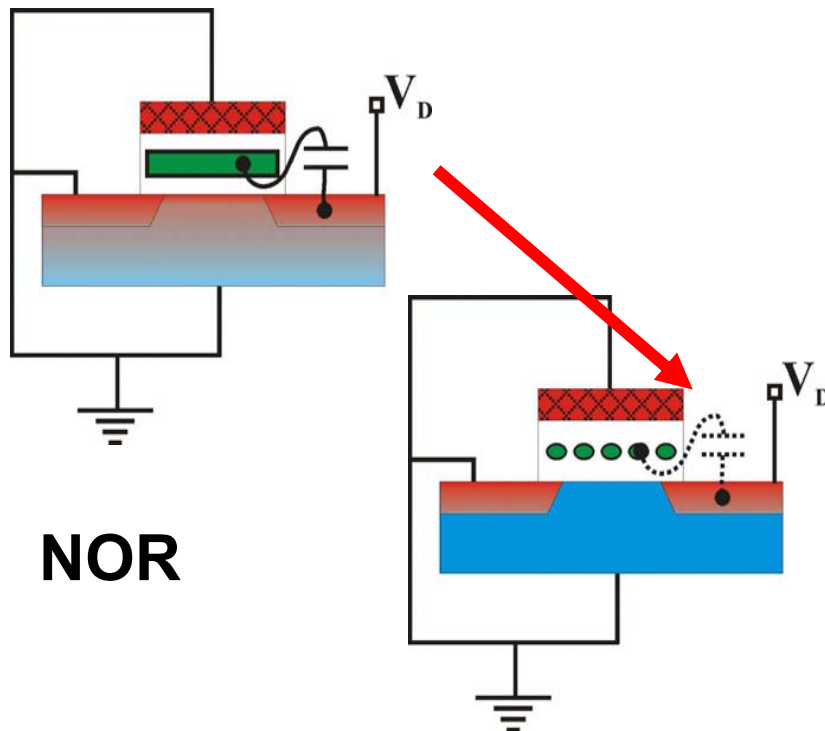
Reduction of tunnel and control oxide thickness
(lower operation voltage for FN tunneling)

Possibility of Multibit storage (like NROM™)

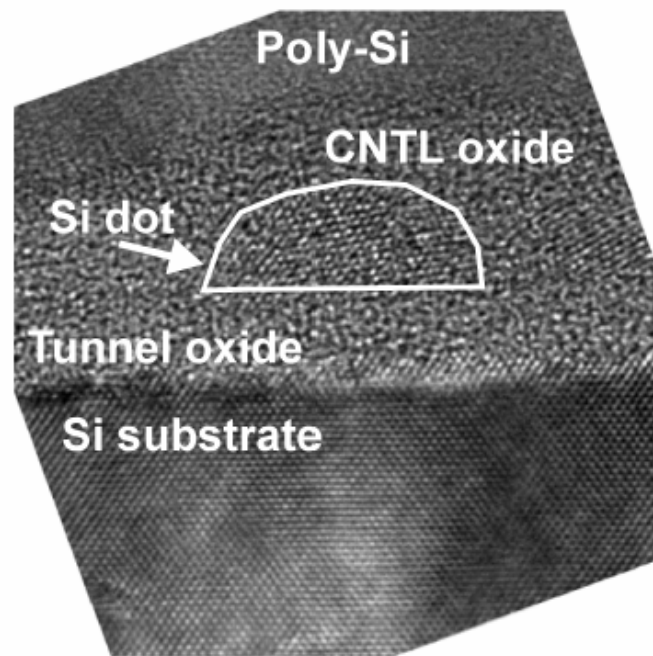


Use of Si dots for charge storage in FLASH

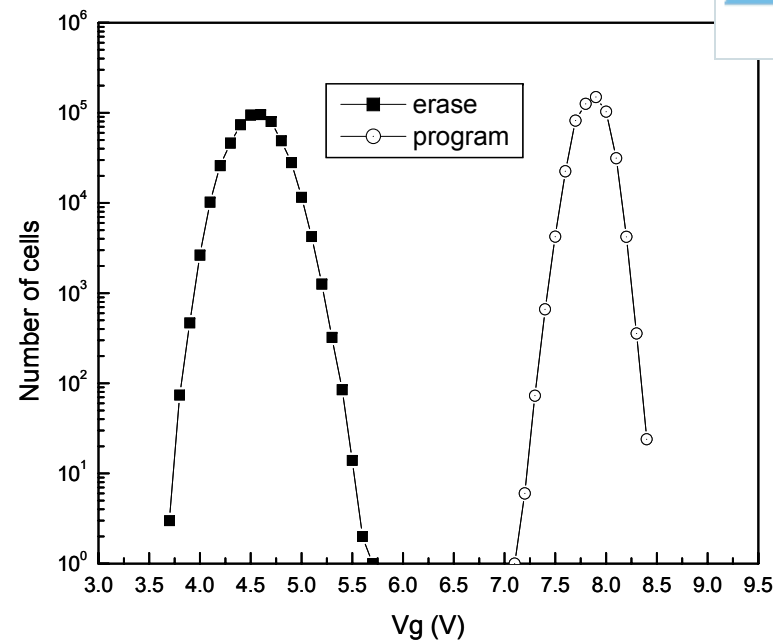
Reduced parasitic capacitances due to the FG.
Example: suppression of Drain turn-on effect in
NOR-Flash



Si Nanocrystal Memories (≈ 5 nm Si dots)



130 nm Technology Chip Demonstrator of Nanocrystal Memory (*)



(*) Nanocrystal Memory Cell Integration in a Stand-Alone 16-Mb nor Flash Device Gerardi, C.; Ancarani, V.; Portoghese, R.; Giuffrida, S.; Bileci, M.; Bimbo, G.; Brafa, O.; Mello, D.; Ammendola, G.; Tripiciano, E.; Puglisi, R.; Lombardo, S.A.; Electron Devices, IEEE Transactions on Volume: 54 , Issue: 6 Publication Year: 2007 , Page(s): 1376 - 1383

Performance and reliability of a 4Mb Si nanocrystal NOR Flash memory with optimized 1T memory cells, Gerardi, C.; Molas, G.; Albini, G.; Tripiciano, E.; Gely, M.; Emmi, A.; Fiore, O.; Nowak, E.; Mello, D.; Vecchio, M.; Masarotto, L.; Portoghese, R.; De Salvo, B.; Deleonibus, S.; Maurelli, A.; Electron Devices Meeting, 2008. IEDM 2008. IEEE International Publication Year: 2008 , Page(s): 1 - 4

Si Nanocrystal Memories (≈ 5 nm Si dots)

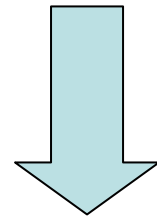
Thin Film Storage (TFS) by  **freescale**[™]

[http://www.freescale.com/webapp/sps/site/overview.jsp
?code=TM_RD_PROCESSTECH_90NMTFS_FLXMEM](http://www.freescale.com/webapp/sps/site/overview.jsp?code=TM_RD_PROCESSTECH_90NMTFS_FLXMEM)

**Freescale's 90nm Thin Film Storage (TFS) flash memory technology
with FlexMemory for 32 bit Microcontrollers**

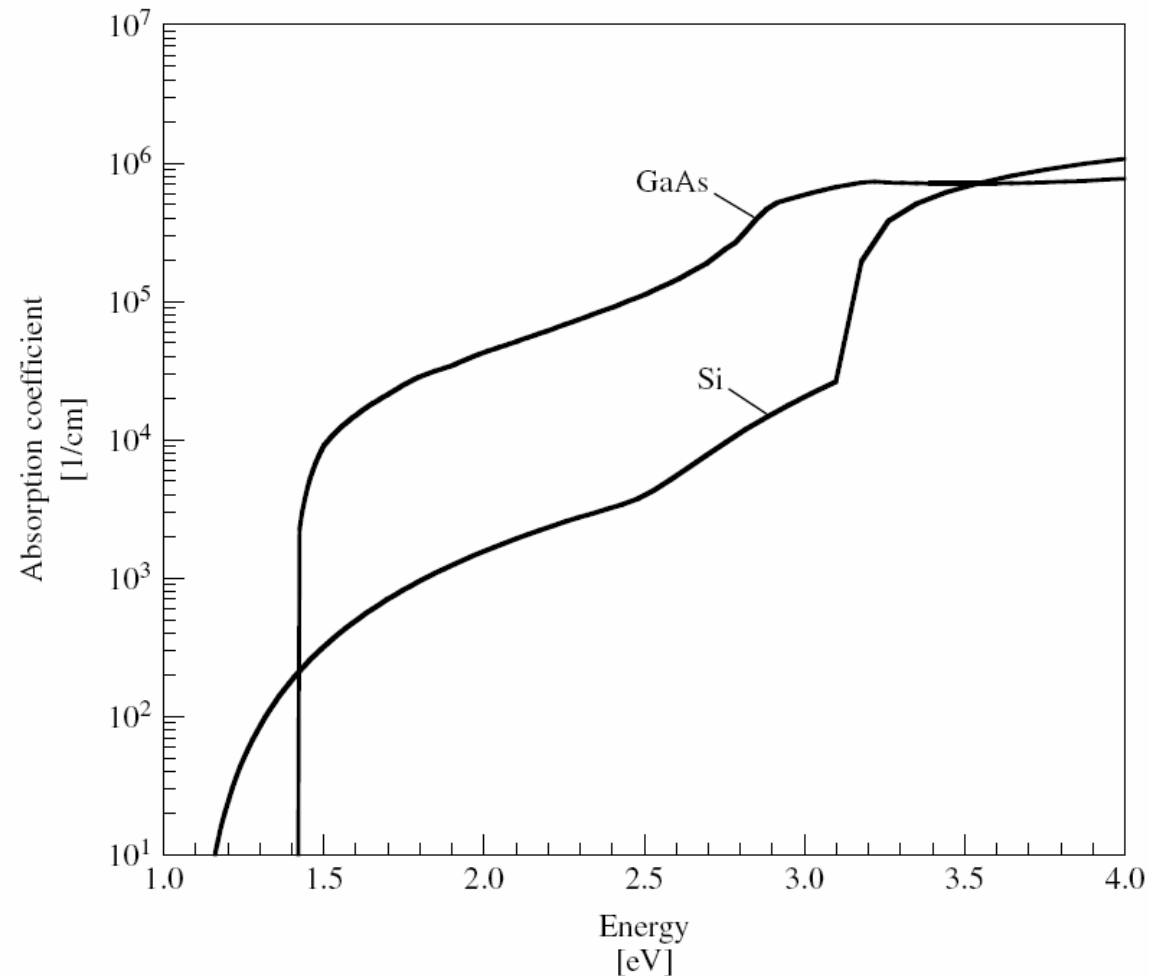


Silicon for Photonics / Photovoltaics

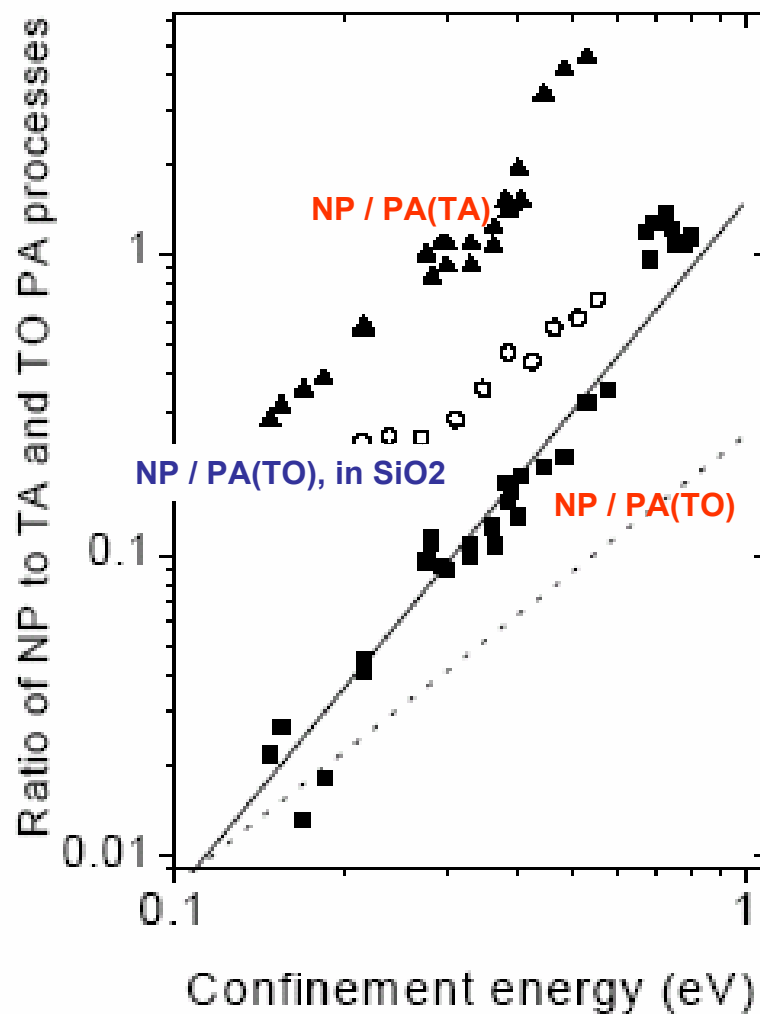
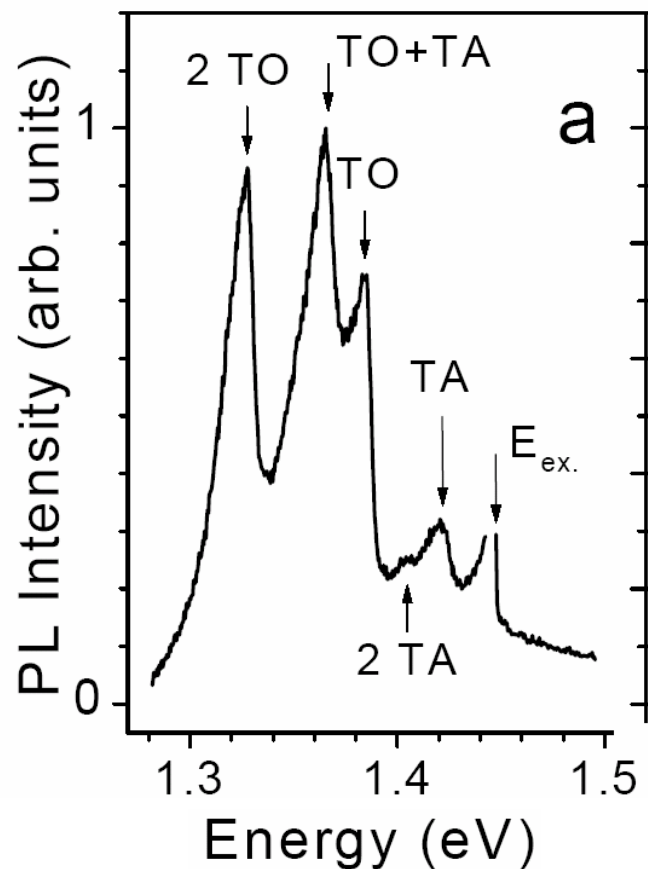


Nanostructures (\approx 1 nm)

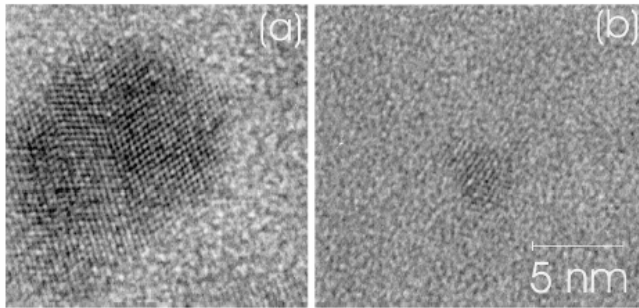
The Challenge of Silicon in this area: Indirect Gap



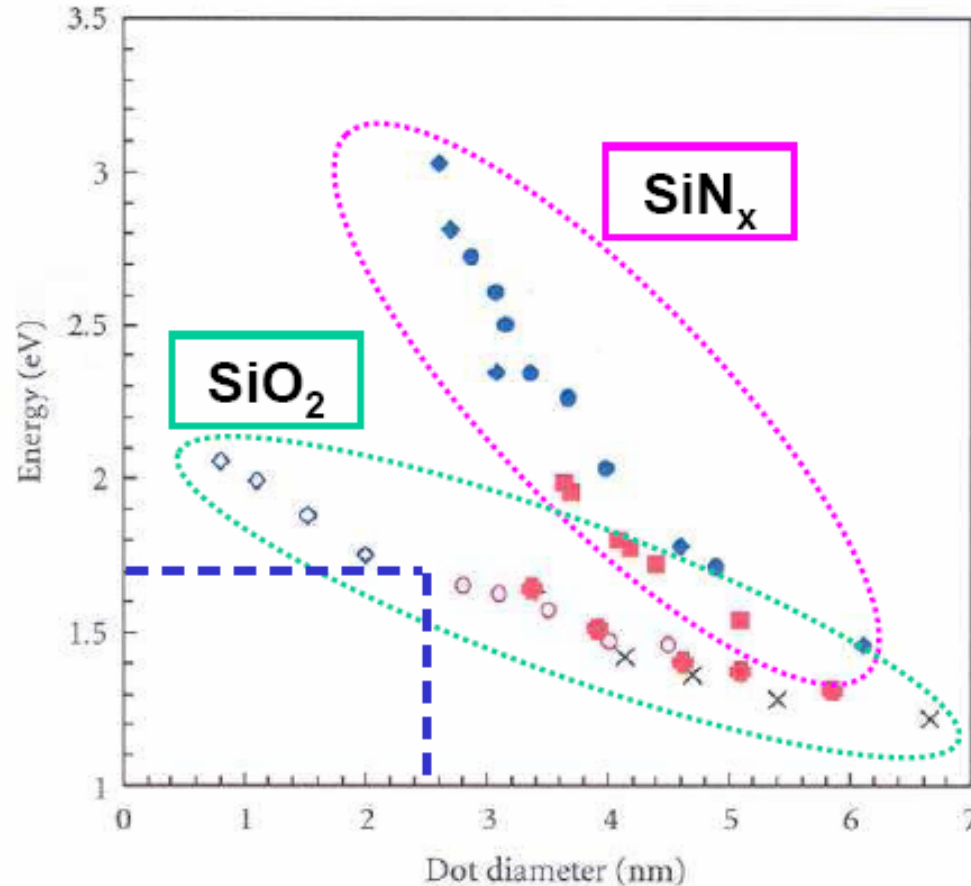
Si Nanocrystals: Breakdown of the k-Conservation Rule



D. Kovalev, PHYSICAL REVIEW LETTERS, 81 (1998)



Si quantum dots: band-gap

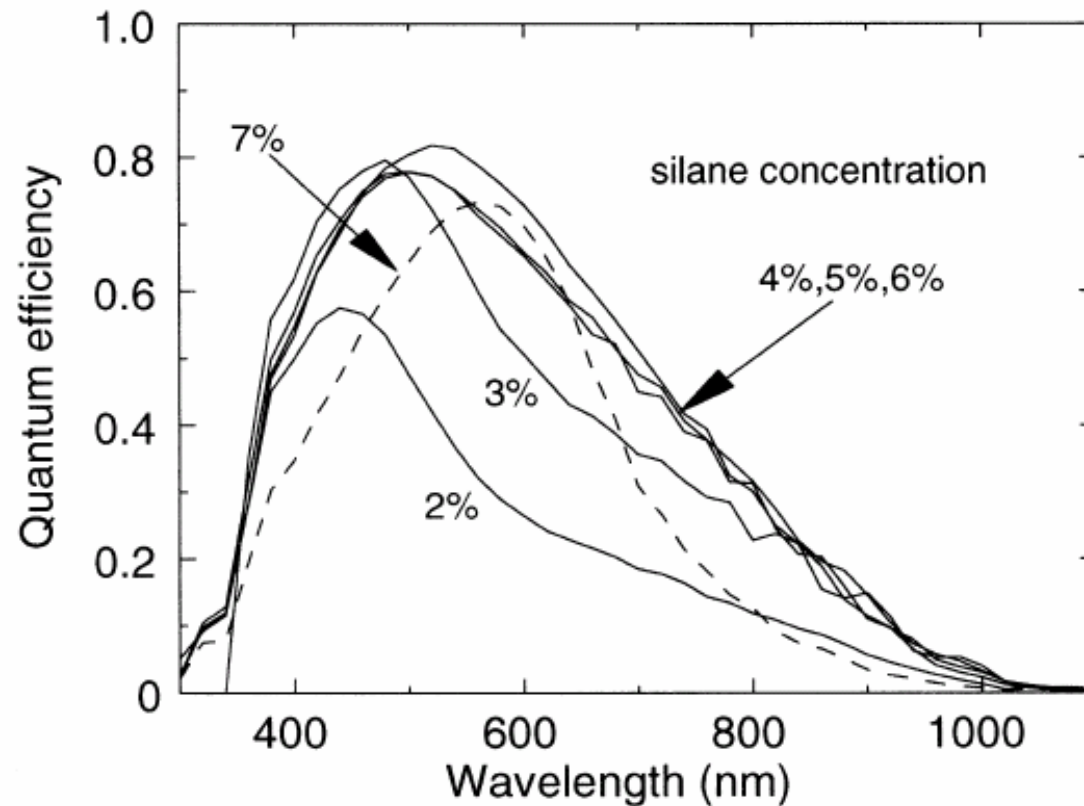


Silicon nanocrystals in SiO₂ and SiN_x
 Photoluminescence measurements
 [Cho, Adv. Optoelectronics (2007)]

**From
 PhotoLuminescence
 Measurements**

- ◇ Y. Kanemitsu et al. [37]
- ◇ H. Takegi et al. [38]
- × S. Takeoka et al. [39]
- ◆ T. Y. Kim et al. [40]
- T. W. Kim et al. [41]
- Oxide (UNSW)
- Nitride (UNSW)

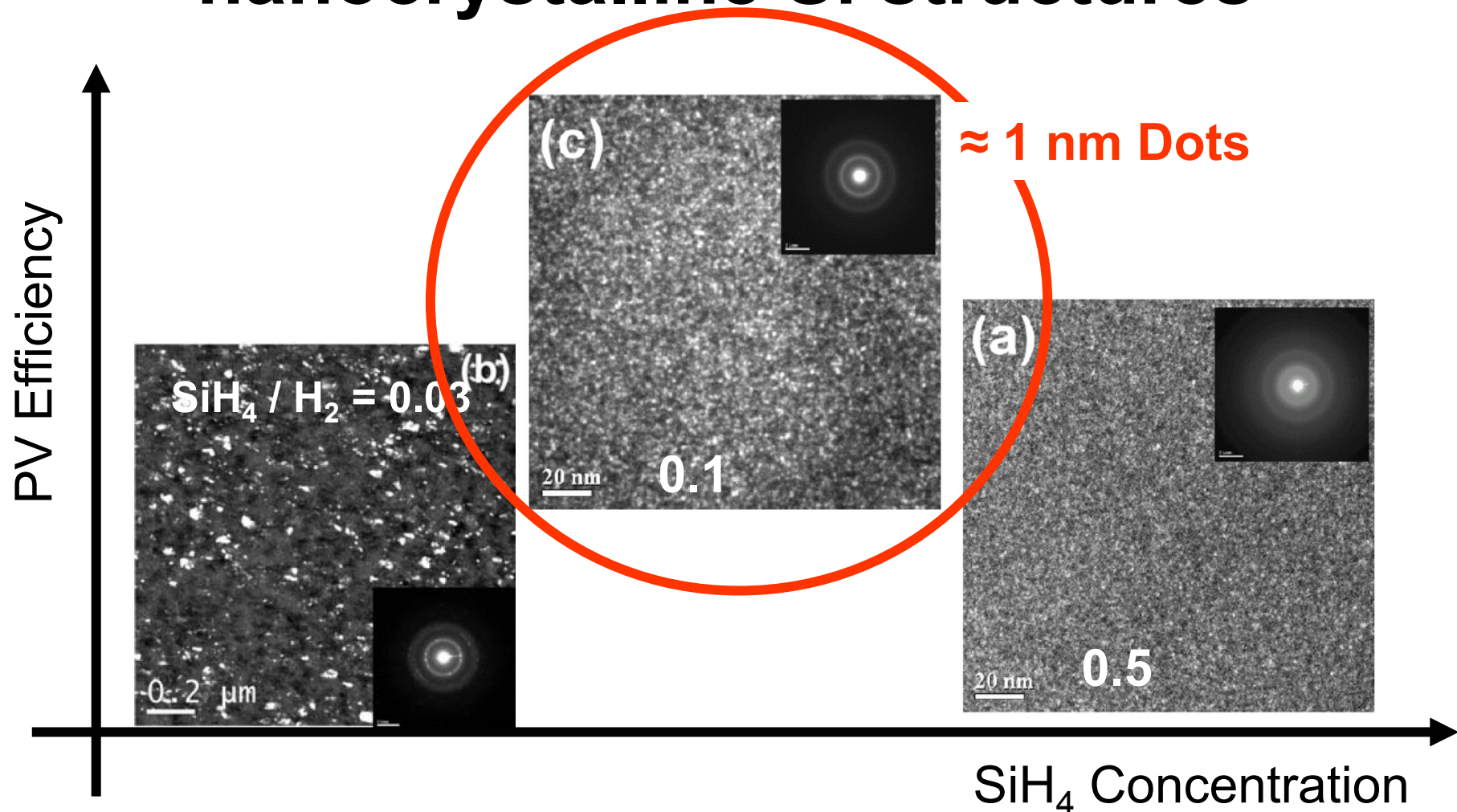
a-Si:H PV cells: the weight of nanostructured Si



**Best efficiency at the boundary
between Crystalline & Amorphous**

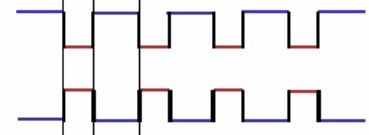
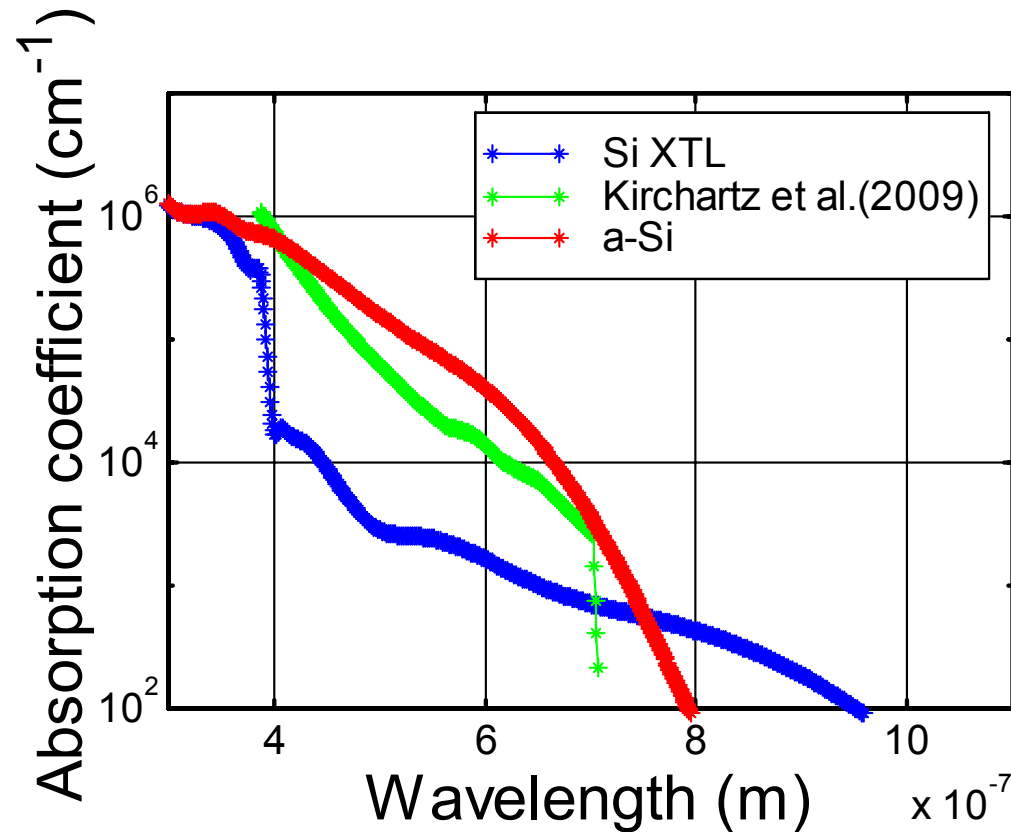
O. Vetterl et al. / Solar Energy Materials & Solar Cells 62 (2000) 97

The boundary phase: Observation of nanocrystalline Si structures



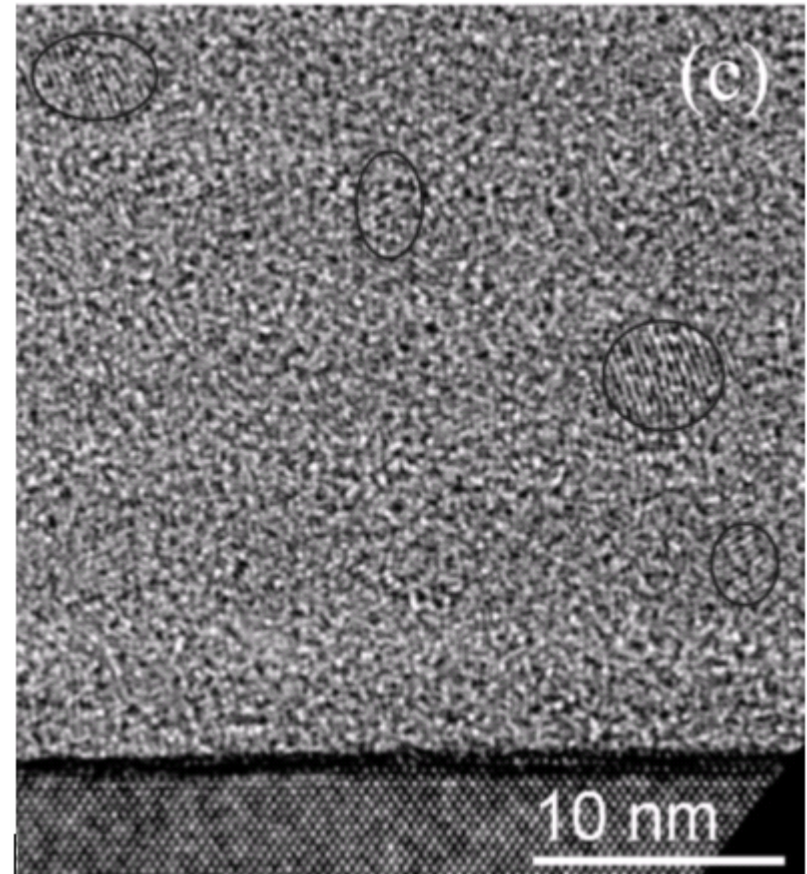
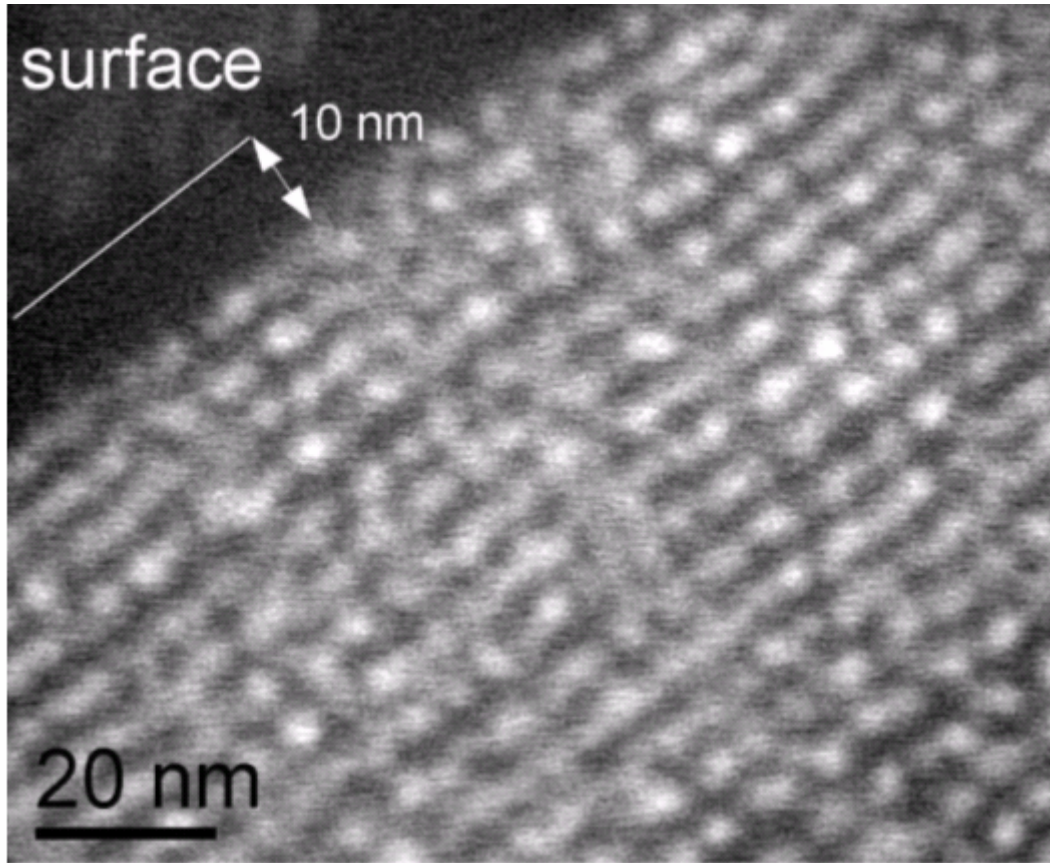
EVOLUTION OF SiH_x HYDRIDES DURING THE PHASE TRANSITION FROM AMORPHOUS TO MICROCRYSTALLINE SILICON FILMS, C. Garozzo, R.A. Puglisi, C. Bongiorno, C. Spinella, S. Mirabella, R. Reitano, S. Di Marco, M. Foti, S. Lombardo, submitted

Absorption Coefficient



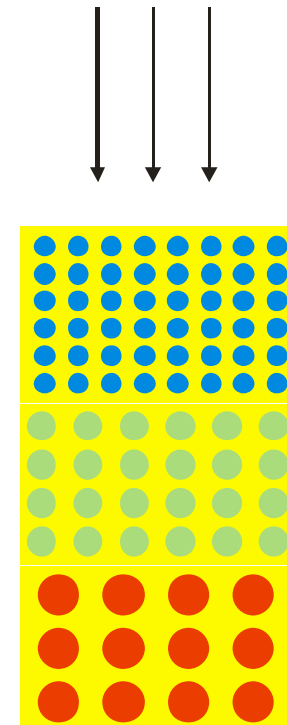
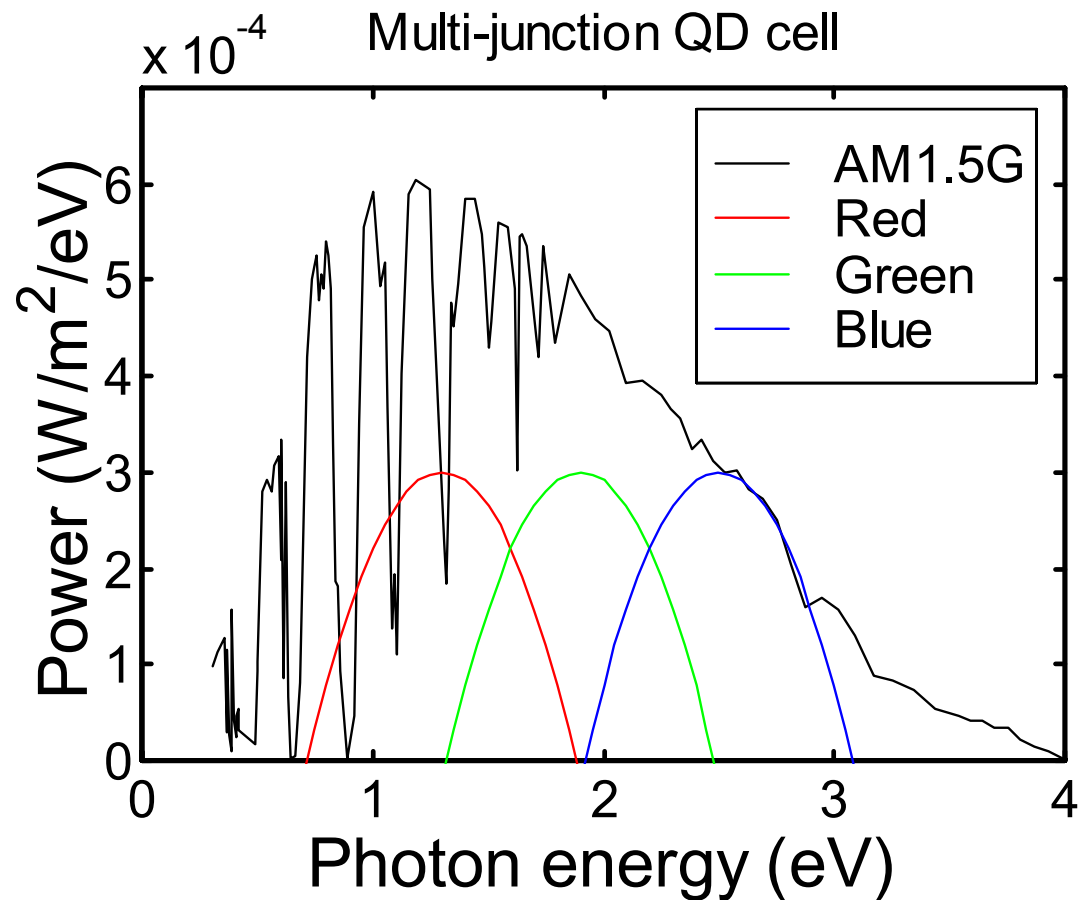
Theory: Kirchartz et al. J. Appl. Phys. 105, 104511 (2009)

SRO / SiO₂ Multilayers

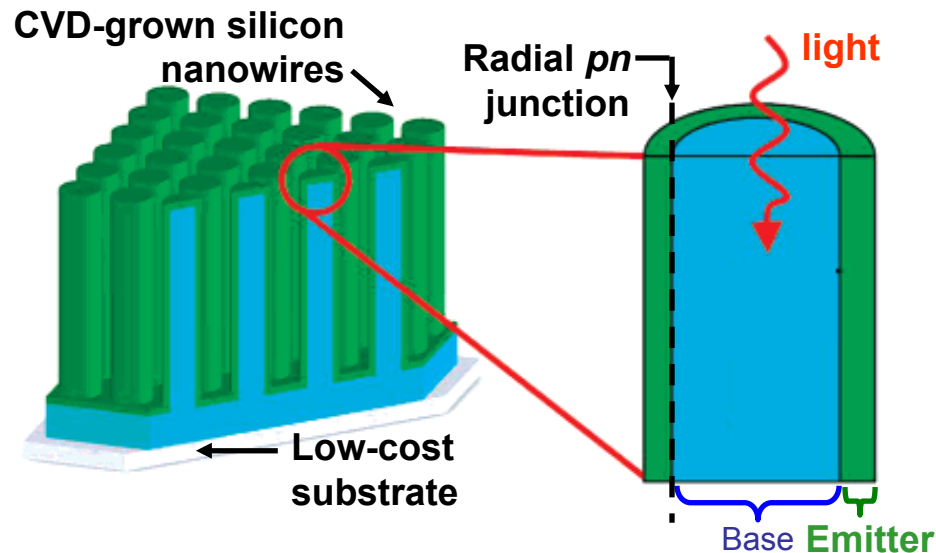


R. A. Puglisi, C. Vecchio, S. Lombardo, S. Lorenti, and M. C. Camalleri, J. Appl. Phys. 108, 023701 2010

Quantum Dot multi-junction PV cells



Silicon nanowire array solar cells



Kayes, J. Appl. Phys. (2005)

Kelzenberg, IEEE PV Specialist Conf. (2008)

- CVD growth of silicon nanowires on glass or metallic substrates
→ **low cost** (similar to thin film technology).
- Radial *pn* junction architecture
→ **high efficiency** ($\approx 15\%$, similar to bulk silicon technology), even for low-quality silicon material.

Summary

Si nanostructures allow tremendous opportunities for **Electronics**

Moore's law, 24 nm now, till the end of the roadmap!

Si nanocrystals memories (≈ 5 nm dots): possible tunnel and control oxide thickness scaling and associated reduction of maximum program / erase voltage and parasitic capacitances.

Photonics & Photovoltaics

The challenge: Si nanostructures with very low sizes (≈ 1 nm) needed for transition to direct gap

Great Opportunities:

- **Energy Harvesting through low cost PV modules**
- **Enhance Photodetector performances**
- **Etc.**